Model Name: 8I915P Duo REV2.01

SHEET	TITLE
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B
06	P4_LGA775_C
07	P4_LGA775_D
08	VCORE POWER
09	GMCH-GRANTSDALE_HOST
10	GMCH-GARNTSDALE_DDR
11	GMCH-GRANTSDALE_PCI E, DMI
12	GMCH-GRANTSDALE_INT VGA
13	GMCH-GRANTSDALE_GND
14	GMCH-GRANTSDALE_PWR
15	DDR CHANNEL A
16	DDR CHANNEL B
17	DDR TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH6 PCI, USB, DMI, LAN
20	ICH6 IDE, GPIO, SATA, CTRL
21	ICH6 VCC, GND
22	CLK GEN

SHEET	TITLE
23	PCI SLOT
24	PCI EXPRESS*1 SLOT
25	ITE8712HX
26	HWMO/FAN/FWH BIOS
27	KB_MS/GAME
28	COM/LPT/FDD
29	(FRONT+REAR)USB/RING/IDE
30	AZALIA CODEC ALC880/CMI9880
31	AUDIO JACK
32	LAN BCM5705E/5751
33	LAN BCM5751
34	ATX POWER CONN.
35	ALL POWER
36	1394 TSB43AB23
37	FRONT PANEL/BZ
38	RAID VIA6410
39	RAID IDE CONNECTOR
40	GPIO TABLE
41	RESET TABLE

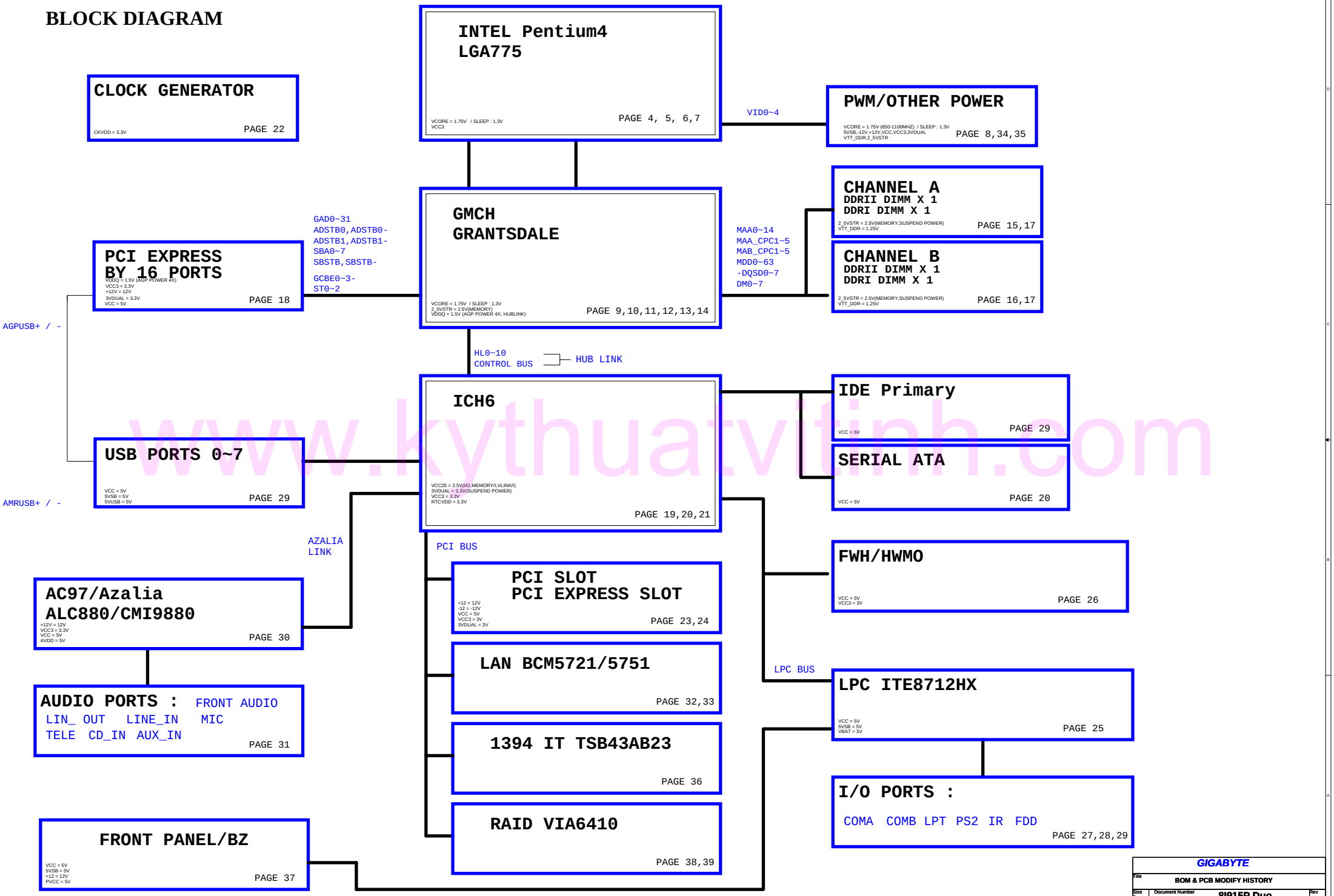
Digitally signed by fdsf
DN: cn=fdsf, o=fsdfsd, ou=ffsdf, email=fdfsd@fsdff, c=US
Date: 2009.12.15 20:38:05 +07'00'

COMPONENT SIDE (1 oz. Copper)
VCC SIDE (1 oz. Copper)
GND SIDE (1 oz. Copper)
SOLDER SIDE (1 oz. Copper)

GIGABYTE

Title	Cover Sheet	
Size: Custom	Document Number: 8I915P Duo	Rev: 2.01
Date: Thursday, April 28, 2005	Sheet 1 of 39	

BLOCK DIAGRAM



GIGABYTE			
Title	BOM & PCB MODIFY HISTORY		
Size: Custom	Document Number: 8I915P Duo		Rev: 2.01
Date: Thursday, April 28, 2005	Sheet 2 of 39		

Model Name: 8I915P Duo
Version: 2.01

Component value change history

2004/11/22

Data	Change Item	Reason
0.1	RELEASE	
1.0	AUDIO2 CHANGE TO 3RJ+15F/[11NR6-403004-31]	
	-RSMRST阻值R1133=22K --> 1K/6	
	CLK-GEN VCC3 BC88,BC91 0.1U/6/Y25V --> 1U/6/Y/10V	
	REMOVE PWROK1 CAP C306=100P & C417=33P	
	PWM DR100 200K --> 178K , DR103 1.8K --> 3.3K , DR82 3.3K --> 3.9K , DR111,112,113 28K --> 39.2K	
	DC32,DC36 CHANGE TO 0.01U/6/X/50V/[10CM1-031002-21_10CM1-031002-27]	
	ADD DDRVTT POWER CAP	
10A-PVT	1. L1,L2 10LI2-00100A-01/02/03 --> 10LI2-12100A-01/02/03	
	2. R563 11K/6/1 --> 20K/6/1	
	3. R565 1.91K/6/1 --> 1.5K/6/1	
	4. U23 10HL6-184148-10 --> 10HL6-184148-20	
10B-0202	1. ADD PWM COMP DC28=180P/4/N/50V	
	2. 加替料U22 SST 49LF003B(10HL4-132003-34)	
	3. ADD RB_MS 替料 10NR6-802006-2A	
20A-0304	1. ADD VT6410 IDE RAID FUNCTION	
20B	1. MANUAL包材加入	
	2. DDR18_0V3電阻修改	
	3. AUDIO2 : 11NR6-403004-71	
915P Duo Rev2.0		
20A-0322	1. 8I915PL-G Rev2.0 --> 8I915P Duo Rev2.0	ADD VT6410 IDE RAID
PVT	1. R1616 5.36K/6/1 --> 6.8K/6/1	
	2. Q193 MMBT2222A --> 2N7002	
20B-0322	1. PCB REv2.0 --> Rev2.01	
	2. Add RN142~RN149 8P4R 33ohm	

Circuit or PCB layout change for next version

PAGE	Change Item	Reason
0.1	EVT	
1.0	PCB 8I915PC DUO Rev0.1 --> 8I915PC DUO Rev1.0	
	ALL 0ohm resister remove , 注意鋪銅	
	CHOKE DL2,DL3,DL4 MODIFY FOOTPRINT=CHOKE06U-40A_1PDL	
	LU1 MARVELL8001 VDD15_L & AVDD25_L ADD 100U/DIP	
	ADD USB PROTECT DIODE	
	ITE8712 GPIO MODIFY FOR OVER VOLTAGE & TURBO PIN	
	LU1 MARVELL8001 PIN8 PIN9不要鋪銅,工廠ICT會SHORT	
	PROCHOT THERMAL RESISTOR REMOVE TO PWM MOSFET	
	背版(ICH6)ICT測試點,保持1.27mm以上	
	CPU PIN/H16 , PIN/U3 未LAUOUT TESTPOINT	
	注意VCC1_5切割 (干擾MCHCLK)	
	BAT SOCKET要改成CO-LAYOUT	
	AUDIO & LAN 之間的AGND,COMP-SOLDER SIDE切開,COMP增加CR32=2.2 ohm	
	PIN HEADER CHECK NEME RULE	
20A-0304	1. ADD VT6410 IDE RAID FUNCTION	
	2. ADD DDR18V_0V3	
	3. ADD BAT RB=1Kohm	
	4. VCC1_5 ADD BC719=0.1U & GATE R1147 2.2 --> 4.7/6	
	5. ADD NEW AVL MOSFET	
915P Duo Rev2.0		
20A-0322	1. 8I915PL-G Rev2.0 --> 8I915P Duo Rev2.0	

GIGABYTE

Title: BOM & PCB MODIFY HISTORY

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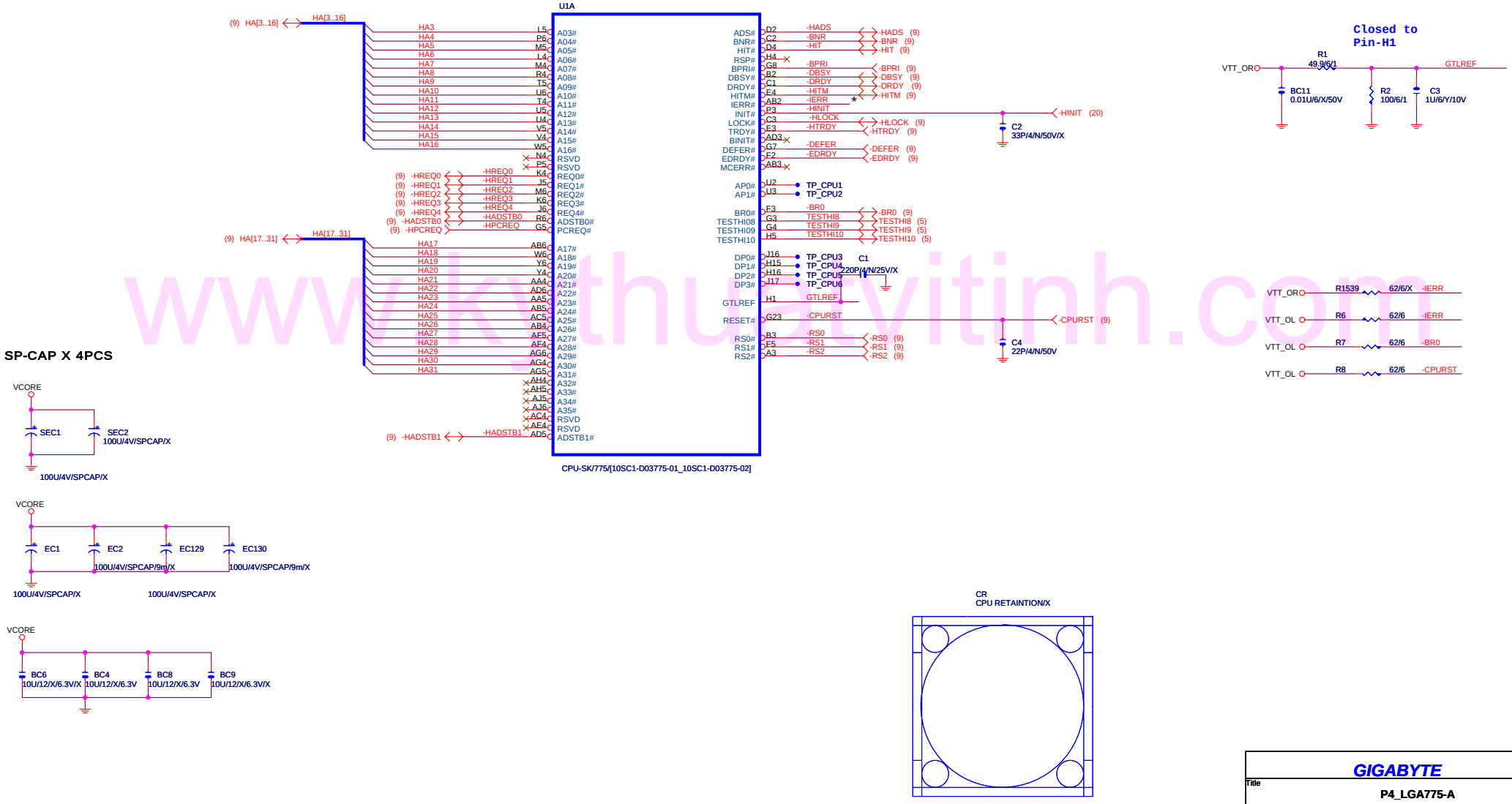
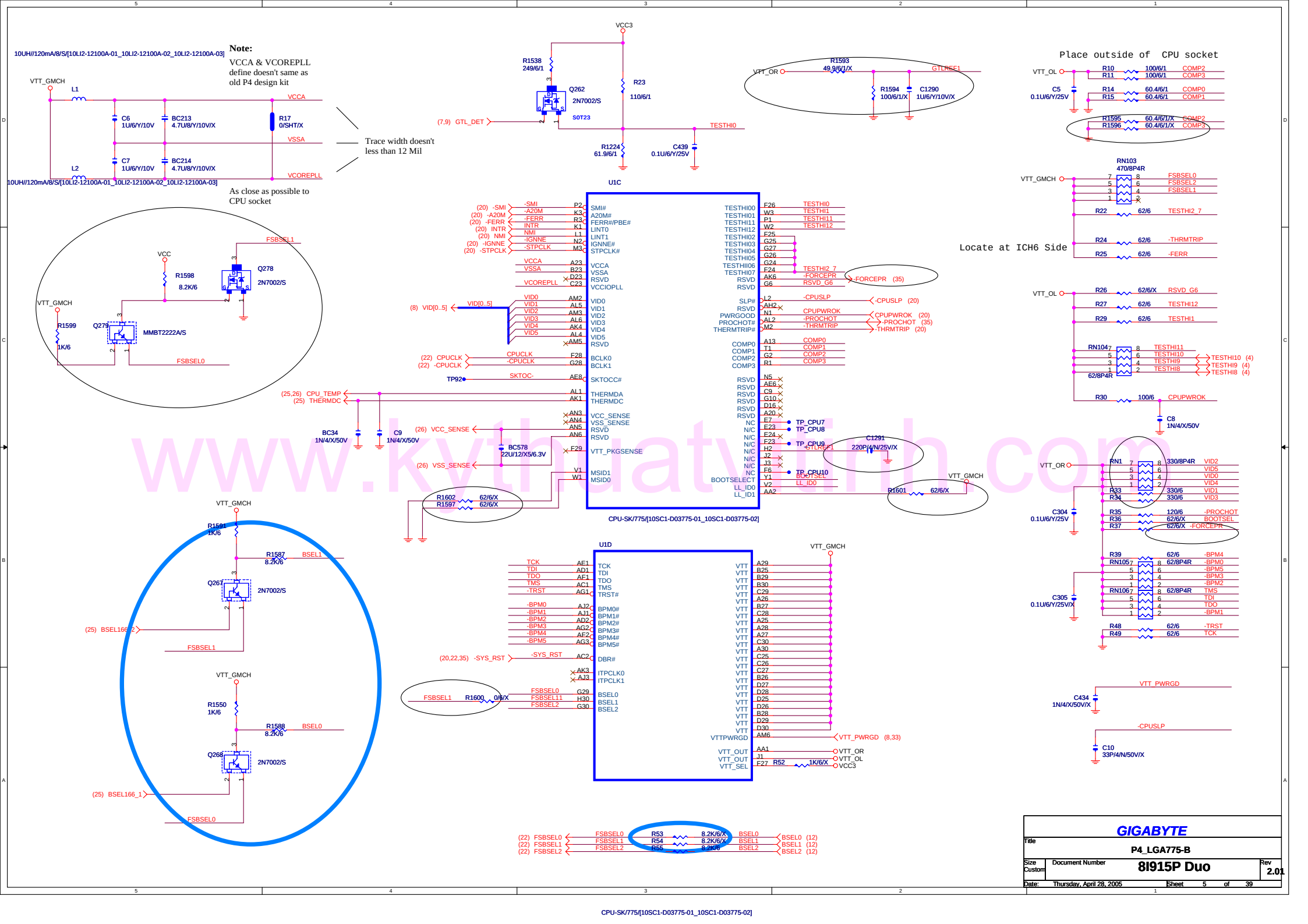
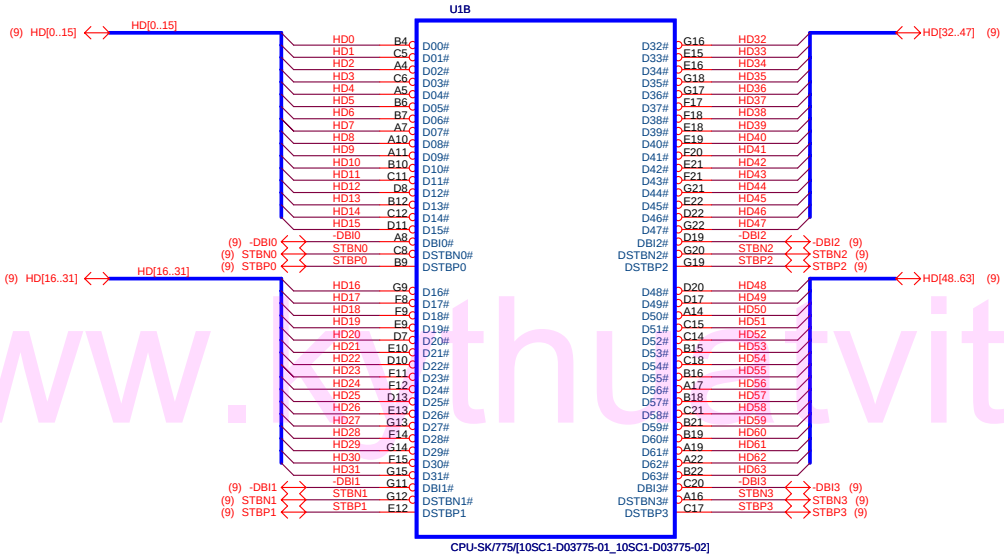
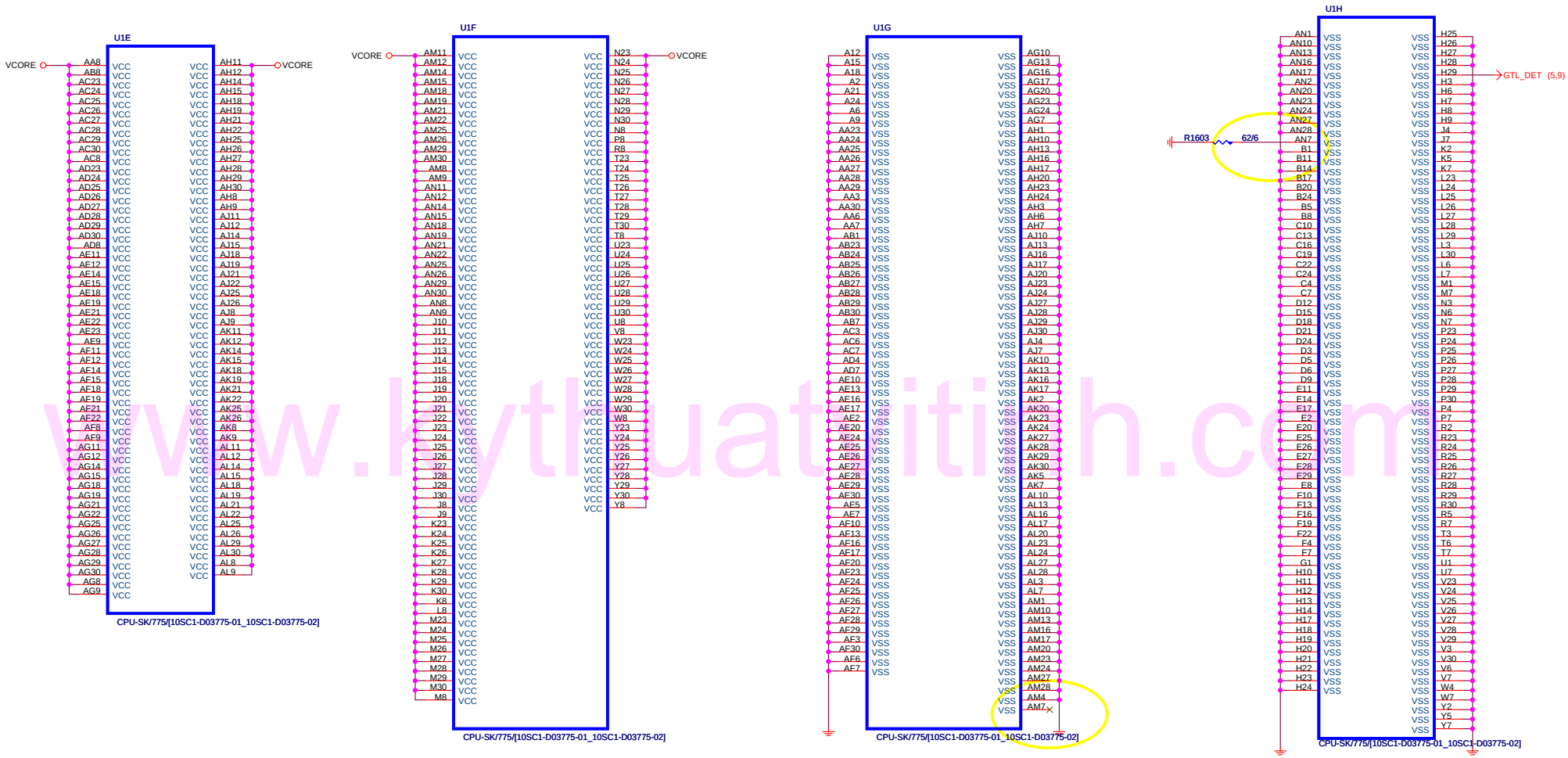


GIGABYTE		
Title	P4_LGA775-A	
Size: Custom	Document Number: 8I915P Duo	Rev: 2.01
Date: Thursday, April 28, 2005	Sheet 4 of 39	

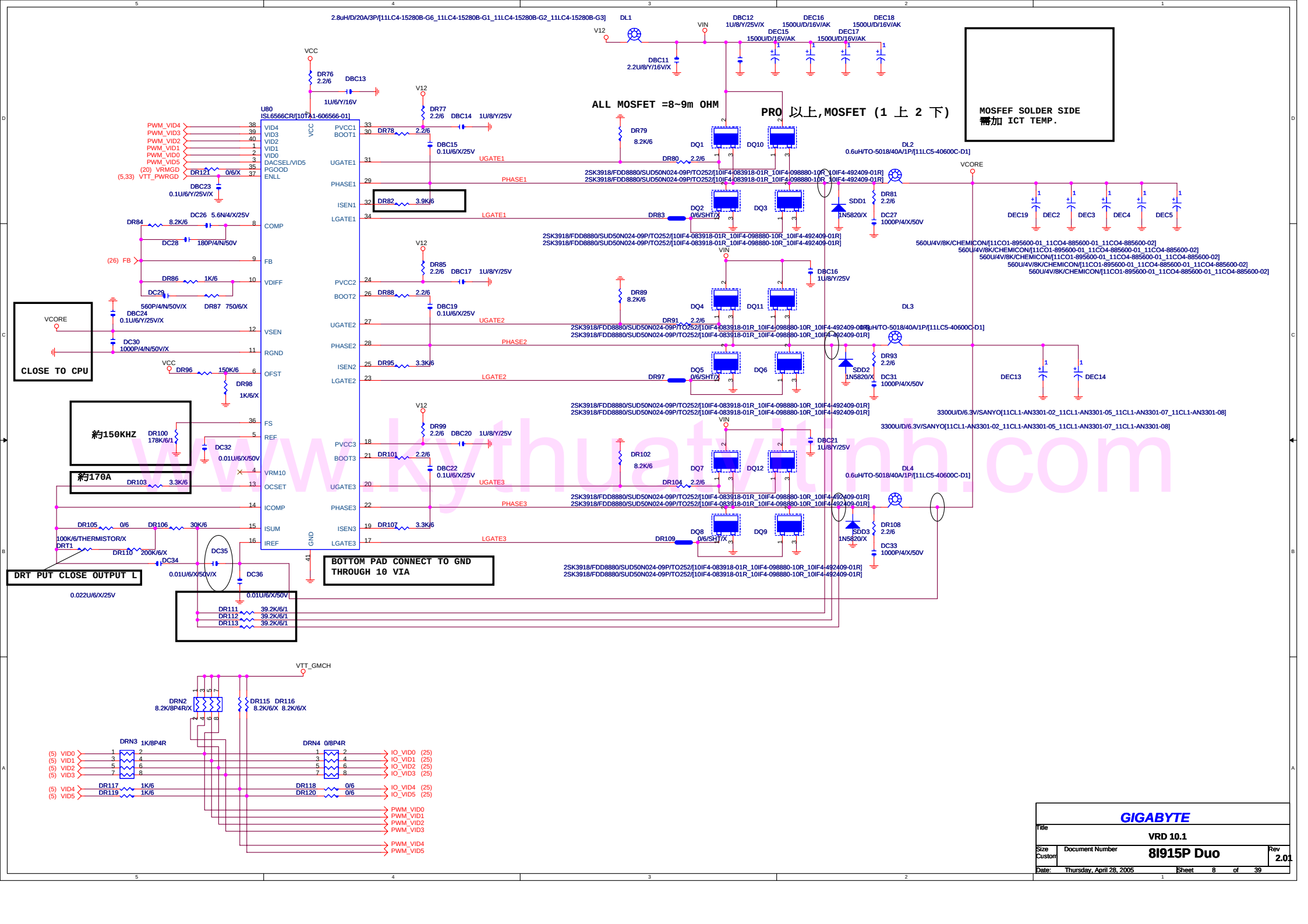


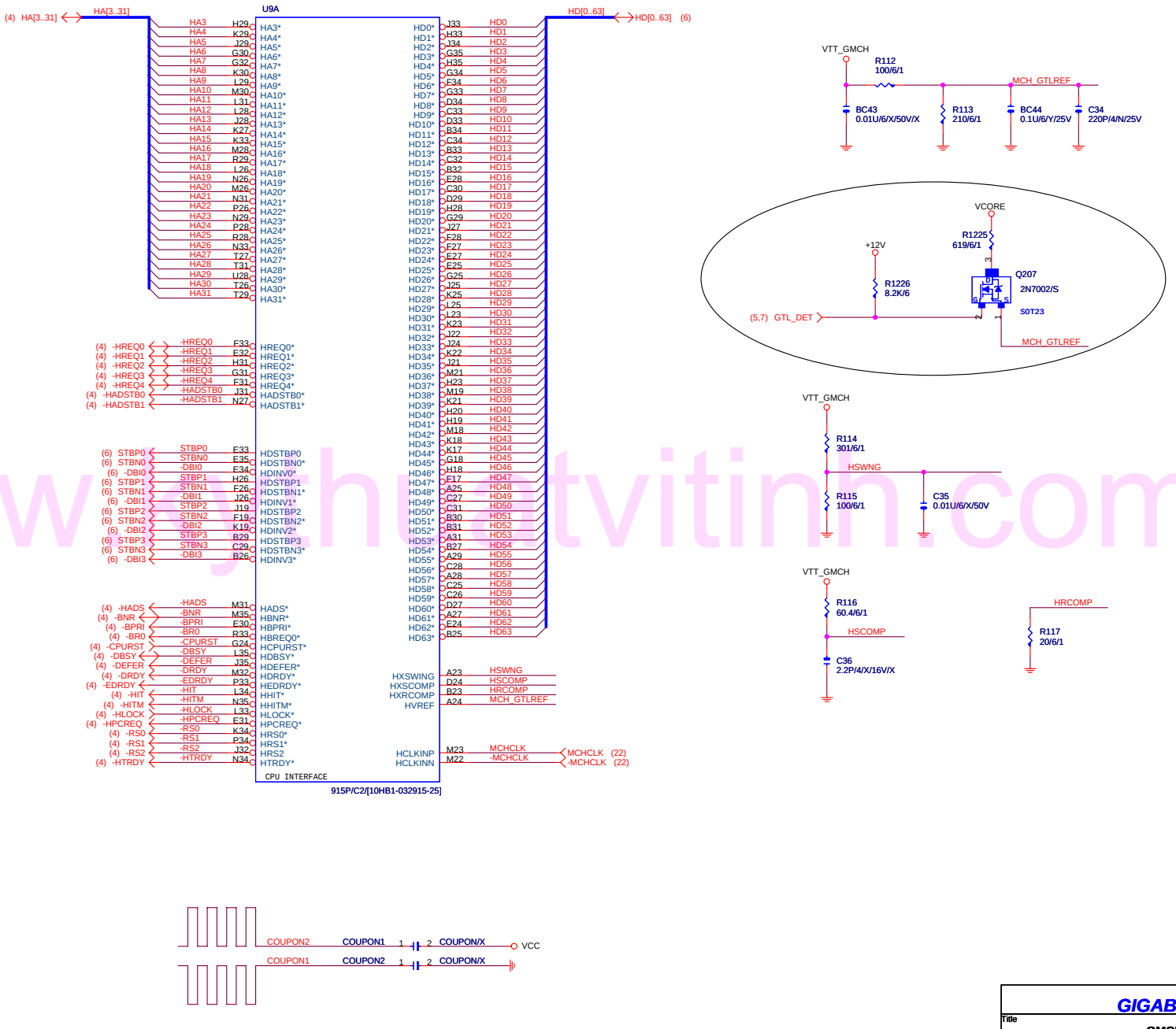


GIGABYTE			
Title: P4_LGA775-C			
Size: Custom	Document Number: 8I915P Duo		Rev: 2.01
Date: Thursday, April 28, 2005	Sheet 6 of 39		

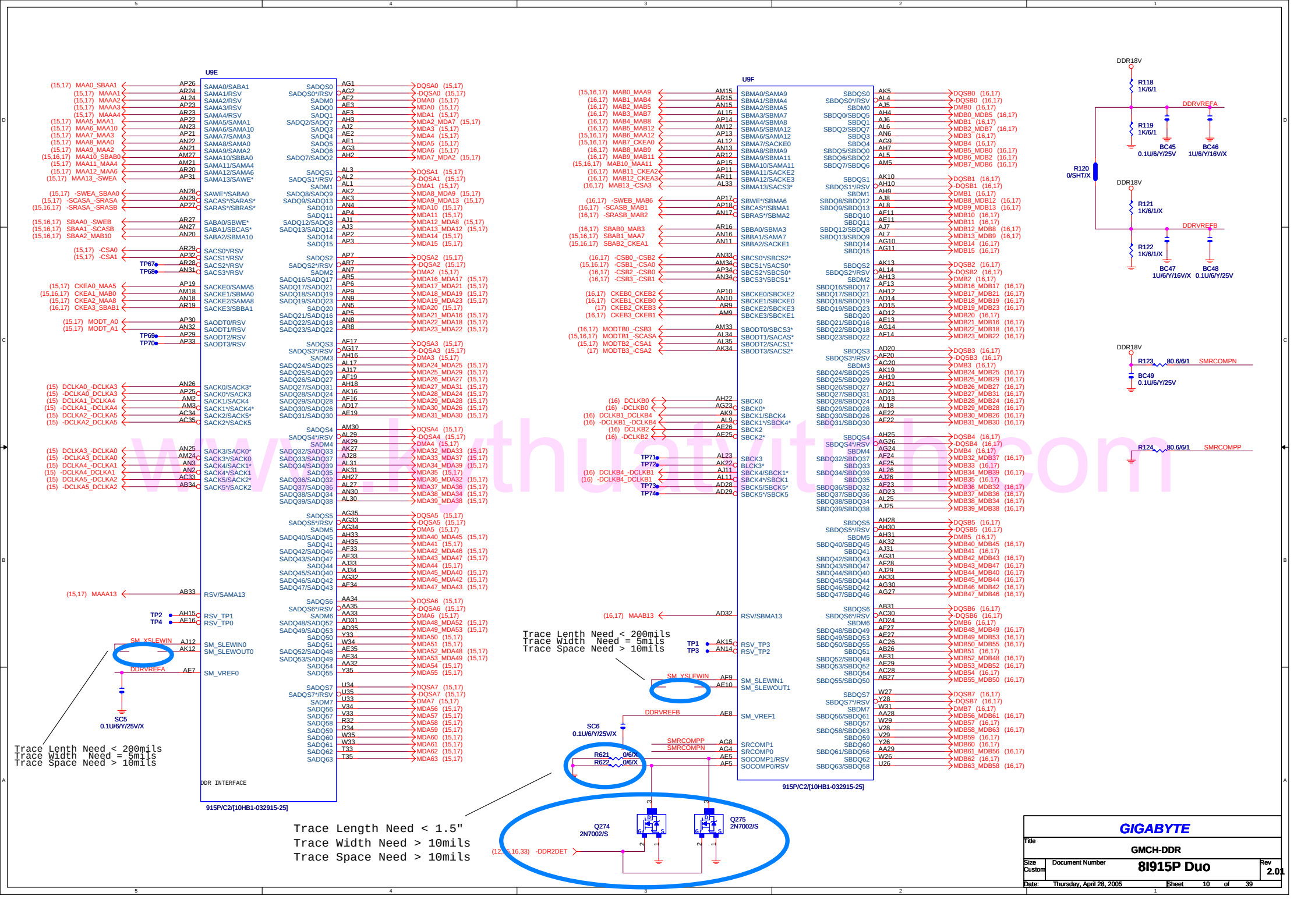


GIGABYTE			
Title	P4_LGA775-D		
Size: Custom	Document Number: 8I915P Duo		Rev: 2.01
Date: Thursday, April 28, 2005	Sheet 7 of 39		





GIGABYTE		
Title	GMCH-HOST	
Size: Custom	Document Number: 8I915P Duo	Rev: 2.01
Date: Thursday, April 28, 2005	Sheet 9 of 39	


U9E
SAMA0/SABA1
SAMA1/RSV
SAMA2/RSV
SAMA3/RSV
SAMA4/RSV
SAMA5/SAMA1
SAMA6/SAMA10
SAMA7/SAMA3
SAMA8/SAMA0
SAMA9/SAMA2
SAMA10/SBBA0
SAMA11/SAMA4
SAMA12/SAMA6
SAMA13/SAWE*
SAWE*/SABA0
SACAS*/SARAS*
SARAS*/SBRAS*
SABA0/SBWE*
SABA1/SBCAS*
SABA2/SBMA10
SACS0*/RSV
SACS1*/RSV
SACS2*/RSV
SACS3*/RSV
SACKE0/SAMA5
SACKE1/SBMA0
SACKE2/SAMA8
SACKE3/SBBA1
SAODT0/RSV
SAODT1/RSV
SAODT2/RSV
SAODT3/RSV
SACK0/SACK3*
SACK0*/SACK3
SACK1/SACK4
SACK1*/SACK4*
SACK2/SACK5*
SACK2*/SACK5
SACK3/SACK0*
SACK3*/SACK0
SACK4/SACK1*
SACK4*/SACK1
SACK5/SACK2*
SACK5*/SACK2
RSV/SAMA13
RSV_TP1
RSV_TP0
SM_SLEWIN0
SM_SLEWOUT0
SM_VREF0
DDR INTERFACE
915P/C2/[10HB1-032915-25]
SADQS0
SADQS0*/RSV
SADM0
SADQ0
SADQ1
SADQ2/SADQ7
SADQ3
SADQ4
SADQ5
SADQ6
SADQ7/SADQ2
SADQS1
SADQS1*/RSV
SADM1
SADQ8/SADQ9
SADQ9/SADQ13
SADQ10
SADQ11
SADQ12/SADQ8
SADQ13/SADQ12
SADQ14
SADQ15
SADQS2
SADQS2*/RSV
SADM2
SADQ16/SADQ17
SADQ17/SADQ21
SADQ18/SADQ19
SADQ19/SADQ23
SADQ20
SADQ21/SADQ16
SADQ22/SADQ18
SADQ23/SADQ22
SADQS3
SADQS3*/RSV
SADM3
SADQ24/SADQ25
SADQ25/SADQ29
SADQ26/SADQ27
SADQ27/SADQ31
SADQ28/SADQ24
SADQ29/SADQ28
SADQ30/SADQ26
SADQ31/SADQ30
SADQS4
SADQS4*/RSV
SADM4
SADQ32/SADQ33
SADQ33/SADQ37
SADQ34/SADQ39
SADQ35
SADQ36/SADQ32
SADQ37/SADQ36
SADQ38/SADQ34
SADQ39/SADQ38
SADQS5
SADQS5*/RSV
SADM5
SADQ40/SADQ45
SADQ41
SADQ42/SADQ46
SADQ43/SADQ47
SADQ44
SADQ45/SADQ40
SADQ46/SADQ42
SADQ47/SADQ43
SADQS6
SADQS6*/RSV
SADM6
SADQ48/SADQ52
SADQ49/SADQ53
SADQ50
SADQ51
SADQ52/SADQ48
SADQ53/SADQ49
SADQ54
SADQ55
SADQS7
SADQS7*/RSV
SADM7
SADQ56
SADQ57
SADQ58
SADQ59
SADQ60
SADQ61
SADQ62
SADQ63
DQSA0 (15,17)
-DQSA0 (15,17)
DMA0 (15,17)
MDA0 (15,17)
MDA1 (15,17)
MDA2_MDA7 (15,17)
MDA3 (15,17)
MDA4 (15,17)
MDA5 (15,17)
MDA6 (15,17)
MDA7_MDA2 (15,17)
DQSA1 (15,17)
-DQSA1 (15,17)
DMA1 (15,17)
MDA8_MDA9 (15,17)
MDA9_MDA13 (15,17)
MDA10 (15,17)
MDA11 (15,17)
MDA12_MDA8 (15,17)
MDA13_MDA12 (15,17)
MDA14 (15,17)
MDA15 (15,17)
DQSA2 (15,17)
-DQSA2 (15,17)
DMA2 (15,17)
MDA16_MDA17 (15,17)
MDA17_MDA21 (15,17)
MDA18_MDA19 (15,17)
MDA19_MDA23 (15,17)
MDA20 (15,17)
MDA21_MDA16 (15,17)
MDA22_MDA18 (15,17)
MDA23_MDA22 (15,17)
DQSA3 (15,17)
-DQSA3 (15,17)
DMA3 (15,17)
MDA24_MDA25 (15,17)
MDA25_MDA29 (15,17)
MDA26_MDA27 (15,17)
MDA27_MDA31 (15,17)
MDA28_MDA24 (15,17)
MDA29_MDA28 (15,17)
MDA30_MDA26 (15,17)
MDA31_MDA30 (15,17)
DQSA4 (15,17)
-DQSA4 (15,17)
DMA4 (15,17)
MDA32_MDA33 (15,17)
MDA33_MDA37 (15,17)
MDA34_MDA39 (15,17)
MDA35 (15,17)
MDA36_MDA32 (15,17)
MDA37_MDA36 (15,17)
MDA38_MDA34 (15,17)
MDA39_MDA38 (15,17)
DQSA5 (15,17)
-DQSA5 (15,17)
DMA5 (15,17)
MDA40_MDA45 (15,17)
MDA41 (15,17)
MDA42_MDA46 (15,17)
MDA43_MDA47 (15,17)
MDA44 (15,17)
MDA45_MDA40 (15,17)
MDA46_MDA42 (15,17)
MDA47_MDA43 (15,17)
DQSA6 (15,17)
-DQSA6 (15,17)
DMA6 (15,17)
MDA48_MDA52 (15,17)
MDA49_MDA53 (15,17)
MDA50 (15,17)
MDA51 (15,17)
MDA52_MDA48 (15,17)
MDA53_MDA49 (15,17)
MDA54 (15,17)
MDA55 (15,17)
DQSA7 (15,17)
-DQSA7 (15,17)
DMA7 (15,17)
MDA56 (15,17)
MDA57 (15,17)
MDA58 (15,17)
MDA59 (15,17)
MDA60 (15,17)
MDA61 (15,17)
MDA62 (15,17)
MDA63 (15,17)
SC5
0.1U/6/Y/25V/X
DDRVREFA
SM_XSLEWIN
Trace Lenth Need < 200mils
Trace Width Need = 5mils
Trace Space Need > 10mils
U9F
SBMA0/SAMA9
SBMA1/SBMA4
SBMA2/SBMA5
SBMA3/SBMA7
SBMA4/SBMA8
SBMA5/SBMA12
SBMA6/SAMA12
SBMA7/SACKE0
SBMA8/SBMA9
SBMA9/SBMA11
SBMA10/SAMA11
SBMA11/SACKE2
SBMA12/SACKE3
SBMA13/SACS3*
SBWE*/SBMA6
SBCAS*/SBMA1
SBRAS*/SBMA2
SBBA0/SBMA3
SBBA1/SAMA7
SBBA2/SACKE1
SBCS0*/SBCS2*
SBCS1*/SACS0*
SBCS2*/SBCS0*
SBCS3*/SBCS1*
SBCKE0/SBCKE2
SBCKE1/SBCKE0
SBCKE2/SBCKE3
SBCKE3/SBCKE1
SBODT0/SBCS3*
SBODT1/SACAS*
SBODT2/SACS1*
SBODT3/SACS2*
SBCK0
SBCK0*
SBCK1/SBCK4
SBCK1*/SBCK4*
SBCK2
SBCK2*
SBCK3
BLCK3*
SBCK4/SBCK1*
SBCK4*/SBCK1
SBCK5/SBCK5*
SBCK5*/SBCK5
RSV/SBMA13
RSV_TP3
RSV_TP2
SM_SLEWIN1
SM_SLEWOUT1
SM_VREF1
SRCOMP1
SRCOMP0
SOCOMP1/RSV
SOCOMP0/RSV
915P/C2/[10HB1-032915-25]
SBDQS0
SBDQS0*/RSV
SBDM0
SBDQ0/SBDQ5
SBDQ1
SBDQ2/SBDQ7
SBDQ3
SBDQ4
SBDQ5/SBDQ0
SBDQ6/SBDQ2
SBDQ7/SBDQ6
SBDQS1
SBDQS1*/RSV
SBDM1
SBDQ8/SBDQ12
SBDQ9/SBDQ13
SBDQ10
SBDQ11
SBDQ12/SBDQ8
SBDQ13/SBDQ9
SBDQ14
SBDQ15
SBDQS2
SBDQS2*/RSV
SBDM2
SBDQ16/SBDQ17
SBDQ17/SBDQ21
SBDQ18/SBDQ19
SBDQ19/SBDQ23
SBDQ20
SBDQ21/SBDQ16
SBDQ22/SBDQ18
SBDQ23/SBDQ22
SBDQS3
SBDQS3*/RSV
SBDM3
SBDQ24/SBDQ25
SBDQ25/SBDQ29
SBDQ26/SBDQ27
SBDQ27/SBDQ31
SBDQ28/SBDQ24
SBDQ29/SBDQ28
SBDQ30/SBDQ26
SBDQ31/SBDQ30
SBDQS4
SBDQS4*/RSV
SBDM4
SBDQ32/SBDQ37
SBDQ33
SBDQ34/SBDQ39
SBDQ35
SBDQ36/SBDQ32
SBDQ37/SBDQ36
SBDQ38/SBDQ34
SBDQ39/SBDQ38
SBDQS5
SBDQS5*/RSV
SBDM5
SBDQ40/SBDQ45
SBDQ41
SBDQ42/SBDQ43
SBDQ43/SBDQ47
SBDQ44/SBDQ40
SBDQ45/SBDQ44
SBDQ46/SBDQ42
SBDQ47/SBDQ46
SBDQS6
SBDQS6*/RSV
SBDM6
SBDQ48/SBDQ49
SBDQ49/SBDQ53
SBDQ50/SBDQ55
SBDQ51
SBDQ52/SBDQ48
SBDQ53/SBDQ52
SBDQ54
SBDQ55/SBDQ50
SBDQS7
SBDQS7*/RSV
SBDM7
SBDQ56/SBDQ61
SBDQ57
SBDQ58/SBDQ63
SBDQ59
SBDQ60
SBDQ61/SBDQ56
SBDQ62
SBDQ63/SBDQ58
DQSB0 (16,17)
-DQSB0 (16,17)
DMB0 (16,17)
MDB0_MDB5 (16,17)
MDB1 (16,17)
MDB2_MDB7 (16,17)
MDB3 (16,17)
MDB4 (16,17)
MDB5_MDB0 (16,17)
MDB6_MDB2 (16,17)
MDB7_MDB6 (16,17)
DQSB1 (16,17)
-DQSB1 (16,17)
DMB1 (16,17)
MDB8_MDB12 (16,17)
MDB9_MDB13 (16,17)
MDB10 (16,17)
MDB11 (16,17)
MDB12_MDB8 (16,17)
MDB13_MDB9 (16,17)
MDB14 (16,17)
MDB15 (16,17)
DQSB2 (16,17)
-DQSB2 (16,17)
DMB2 (16,17)
MDB16_MDB17 (16,17)
MDB17_MDB21 (16,17)
MDB18_MDB19 (16,17)
MDB19_MDB23 (16,17)
MDB20 (16,17)
MDB21_MDB16 (16,17)
MDB22_MDB18 (16,17)
MDB23_MDB22 (16,17)
DQSB3 (16,17)
-DQSB3 (16,17)
DMB3 (16,17)
MDB24_MDB25 (16,17)
MDB25_MDB29 (16,17)
MDB26_MDB27 (16,17)
MDB27_MDB31 (16,17)
MDB28_MDB24 (16,17)
MDB29_MDB28 (16,17)
MDB30_MDB26 (16,17)
MDB31_MDB30 (16,17)
DQSB4 (16,17)
-DQSB4 (16,17)
DMB4 (16,17)
MDB32_MDB37 (16,17)
MDB33 (16,17)
MDB34_MDB39 (16,17)
MDB35 (16,17)
MDB36_MDB32 (16,17)
MDB37_MDB36 (16,17)
MDB38_MDB34 (16,17)
MDB39_MDB38 (16,17)
DQSB5 (16,17)
-DQSB5 (16,17)
DMB5 (16,17)
MDB40_MDB45 (16,17)
MDB41 (16,17)
MDB42_MDB43 (16,17)
MDB43_MDB47 (16,17)
MDB44_MDB40 (16,17)
MDB45_MDB44 (16,17)
MDB46_MDB42 (16,17)
MDB47_MDB46 (16,17)
DQSB6 (16,17)
-DQSB6 (16,17)
DMB6 (16,17)
MDB48_MDB49 (16,17)
MDB49_MDB53 (16,17)
MDB50_MDB55 (16,17)
MDB51 (16,17)
MDB52_MDB48 (16,17)
MDB53_MDB52 (16,17)
MDB54 (16,17)
MDB55_MDB50 (16,17)
DQSB7 (16,17)
-DQSB7 (16,17)
DMB7 (16,17)
MDB56_MDB61 (16,17)
MDB57 (16,17)
MDB58_MDB63 (16,17)
MDB59 (16,17)
MDB60 (16,17)
MDB61_MDB56 (16,17)
MDB62 (16,17)
MDB63_MDB58 (16,17)
SC6
0.1U/6/Y/25V/X
DDRVREFB
SMRCOMPP
SMRCOMPN
R621 0/6/X
R622 0/6/X
Q274
2N7002/S
Q275
2N7002/S
-DDR2DET
Trace Length Need < 1.5"
Trace Width Need > 10mils
Trace Space Need > 10mils
Trace Lenth Need < 200mils
Trace Width Need = 5mils
Trace Space Need > 10mils
DDR18V
R118 1K/6/1
R119 1K/6/1
DDRVREFA
BC45 0.1U/6/Y/25V
BC46 1U/6/Y/16V/X
R120 0/SHT/X
R121 1K/6/1/X
R122 1K/6/1/X
DDRVREFB
BC47 1U/6/Y/16V/X
BC48 0.1U/6/Y/25V
R123 80.6/6/1
SMRCOMPN
BC49 0.1U/6/Y/25V
R124 80.6/6/1
SMRCOMPP
GIGABYTE
Title
GMCH-DDR
Size Custom
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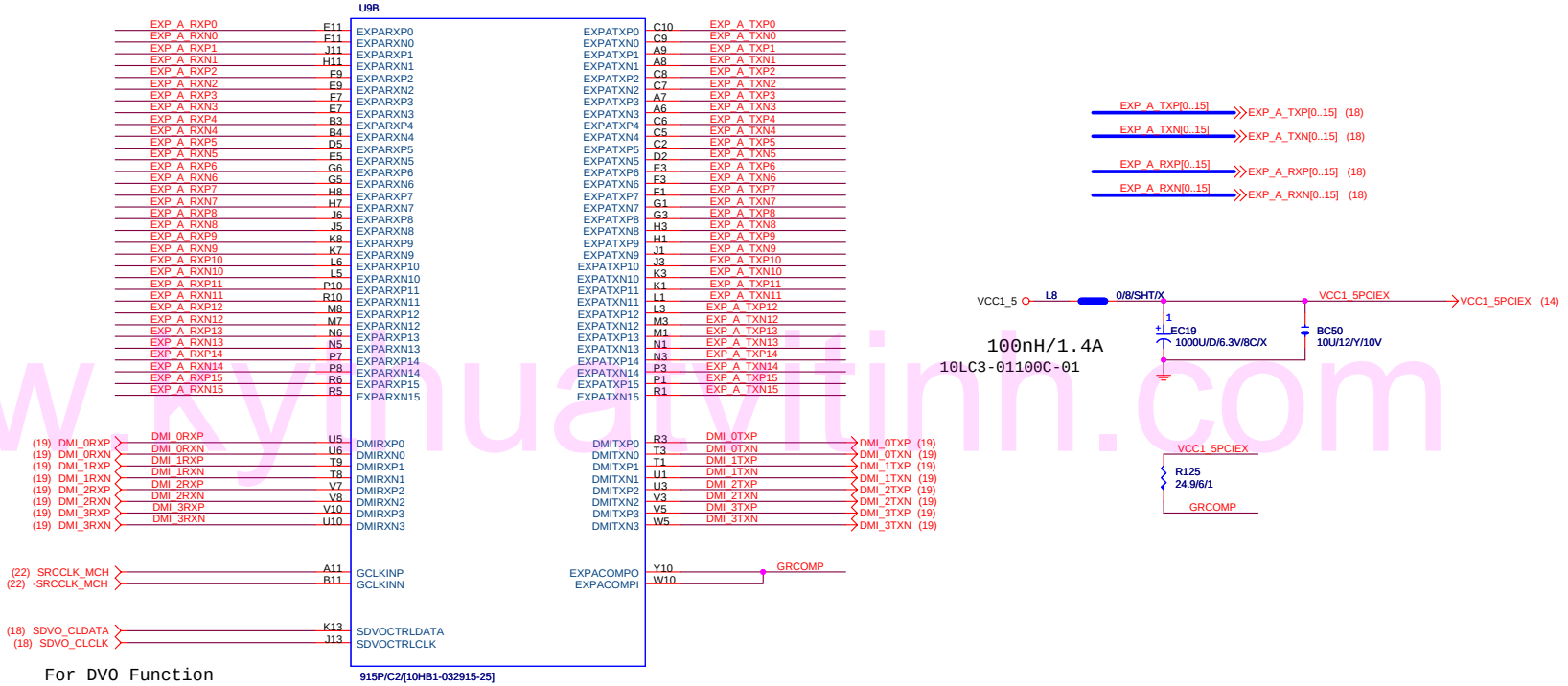

GIGABYTE

Title	GMCH-PCI E & DMI	
Size: Custom	Document Number: 8I915P Duo	Rev: 2.01
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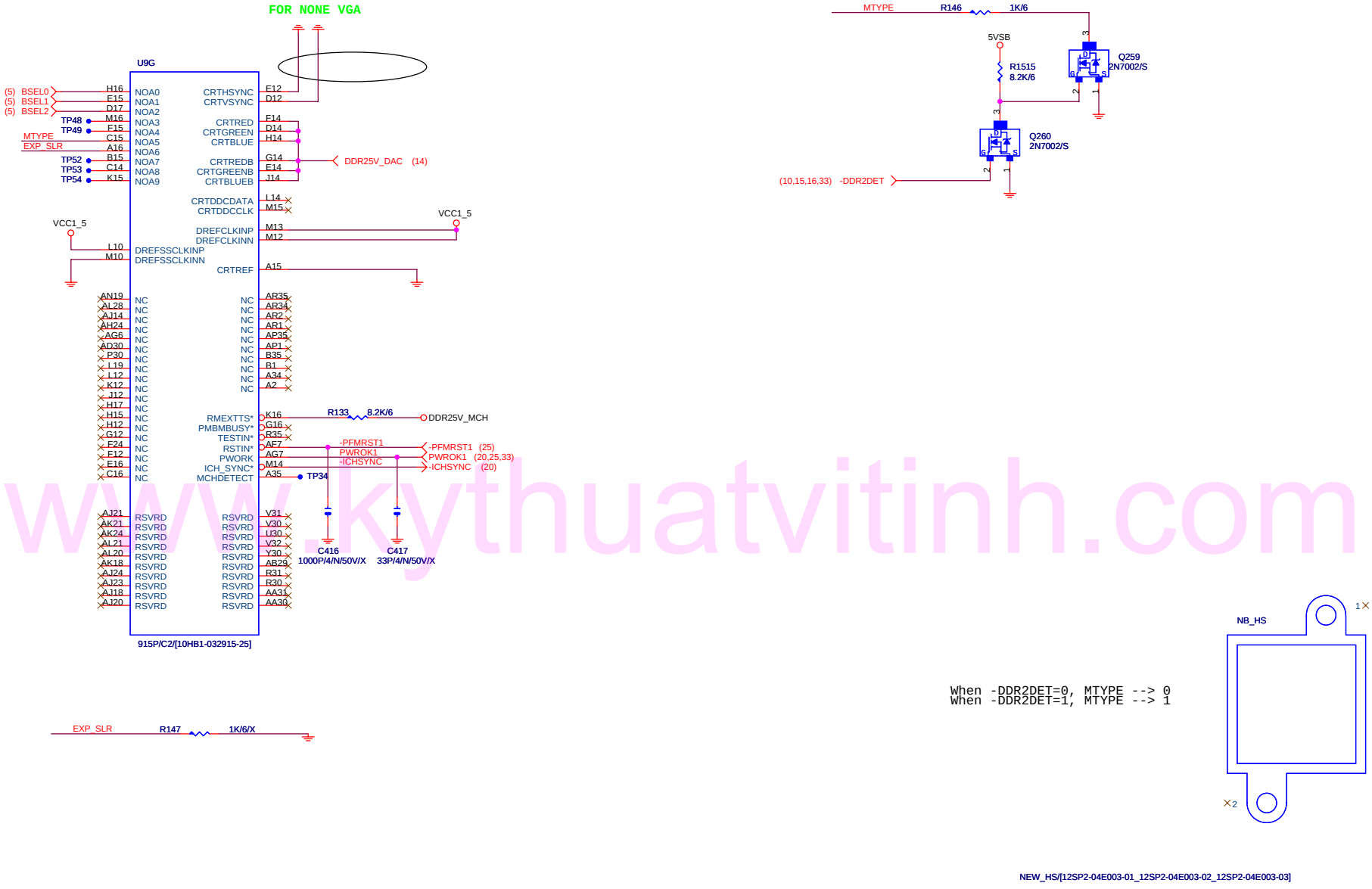

GIGABYTE		
Title	GMCH-INTERNAL VGA	
Size: Custom	Document Number: 8I915P Duo	Rev: 2.01
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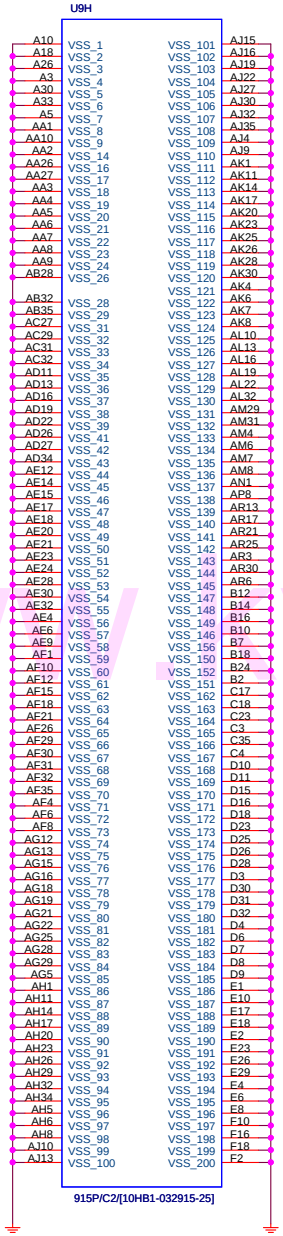

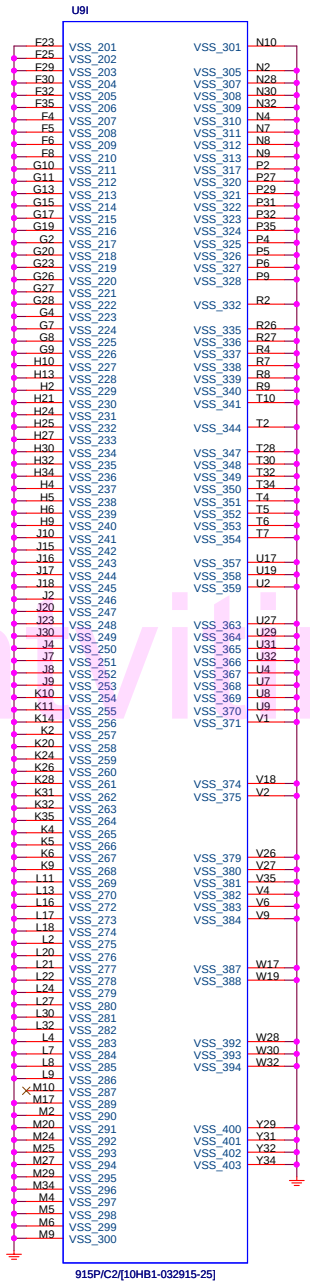

GIGABYTE

Title: GMCH-GND

Size: Custom | Document Number: 8I915P Duo | Rev: 2.01

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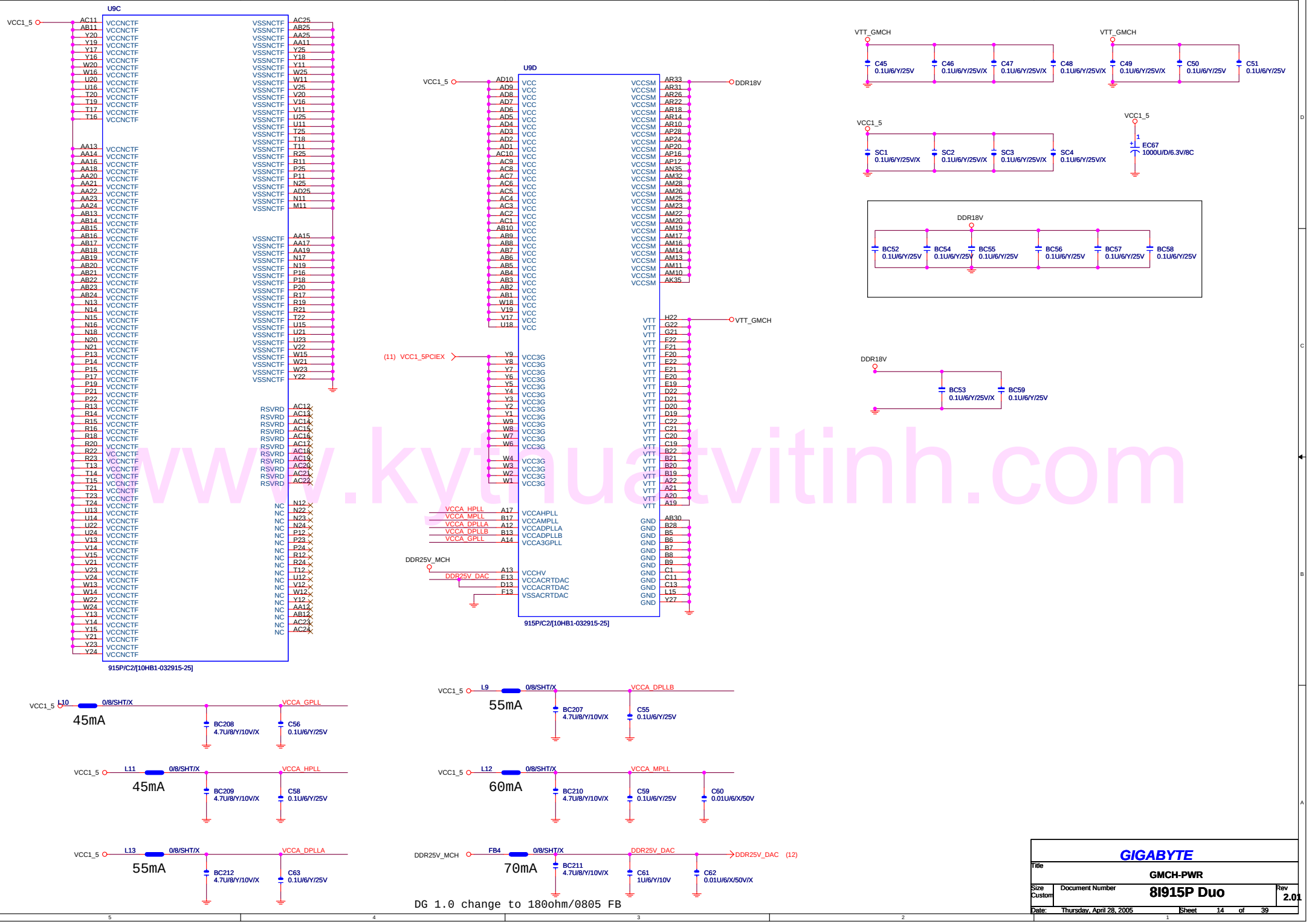

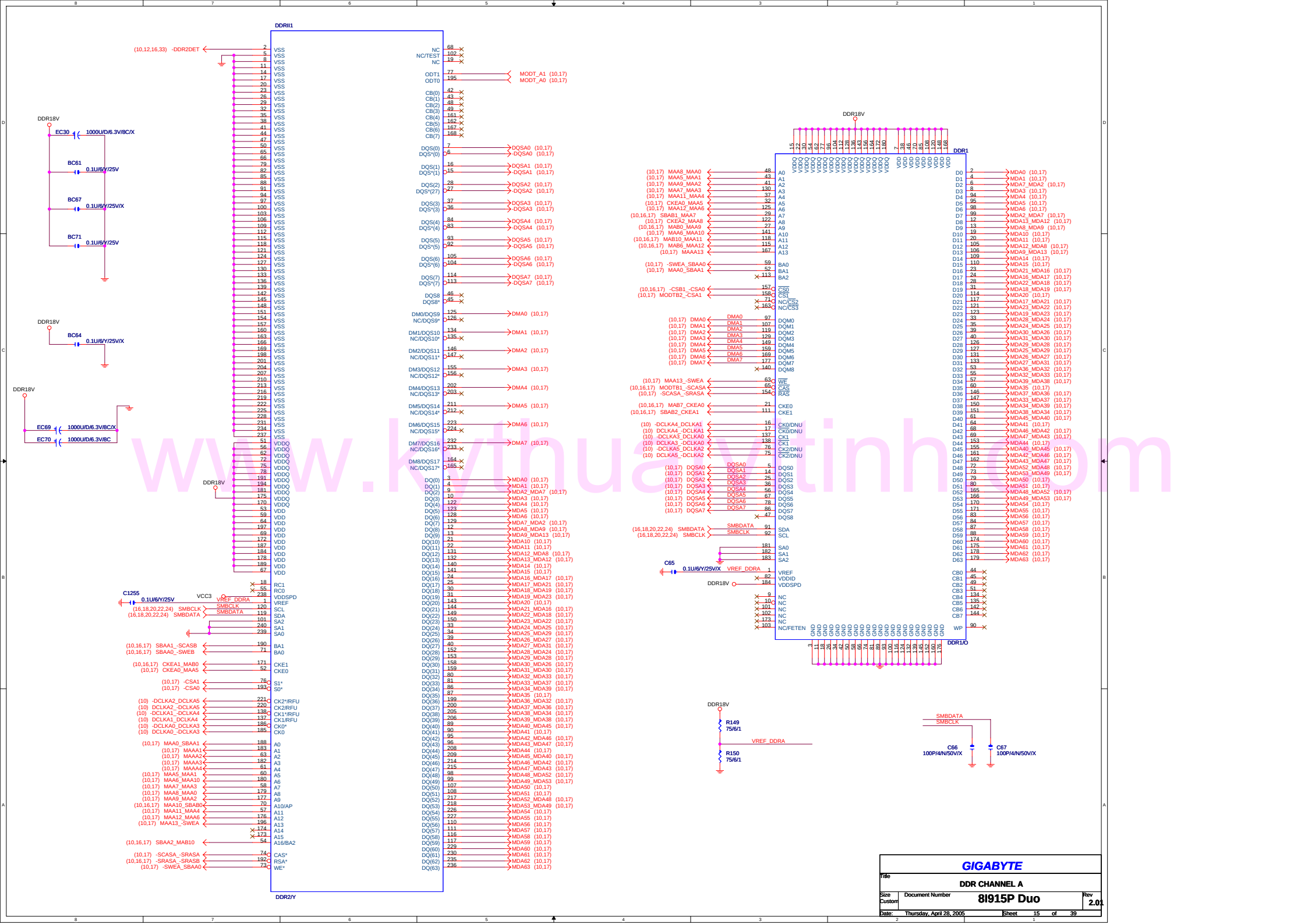

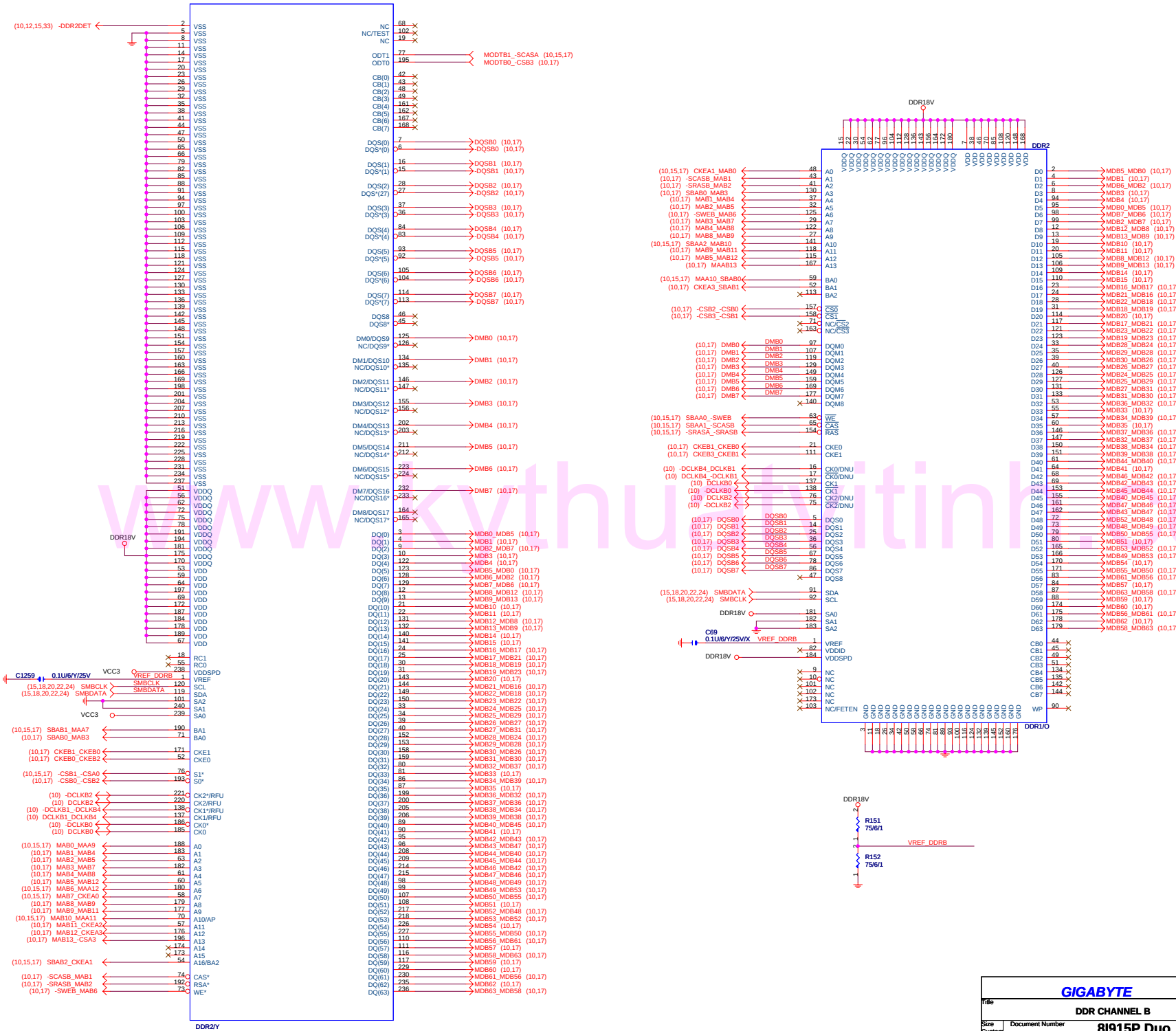

GIGABYTE			
Title	DDR CHANNEL B		
Size: Custom	Document Number: 8I915P Duo		Rev: 2.01
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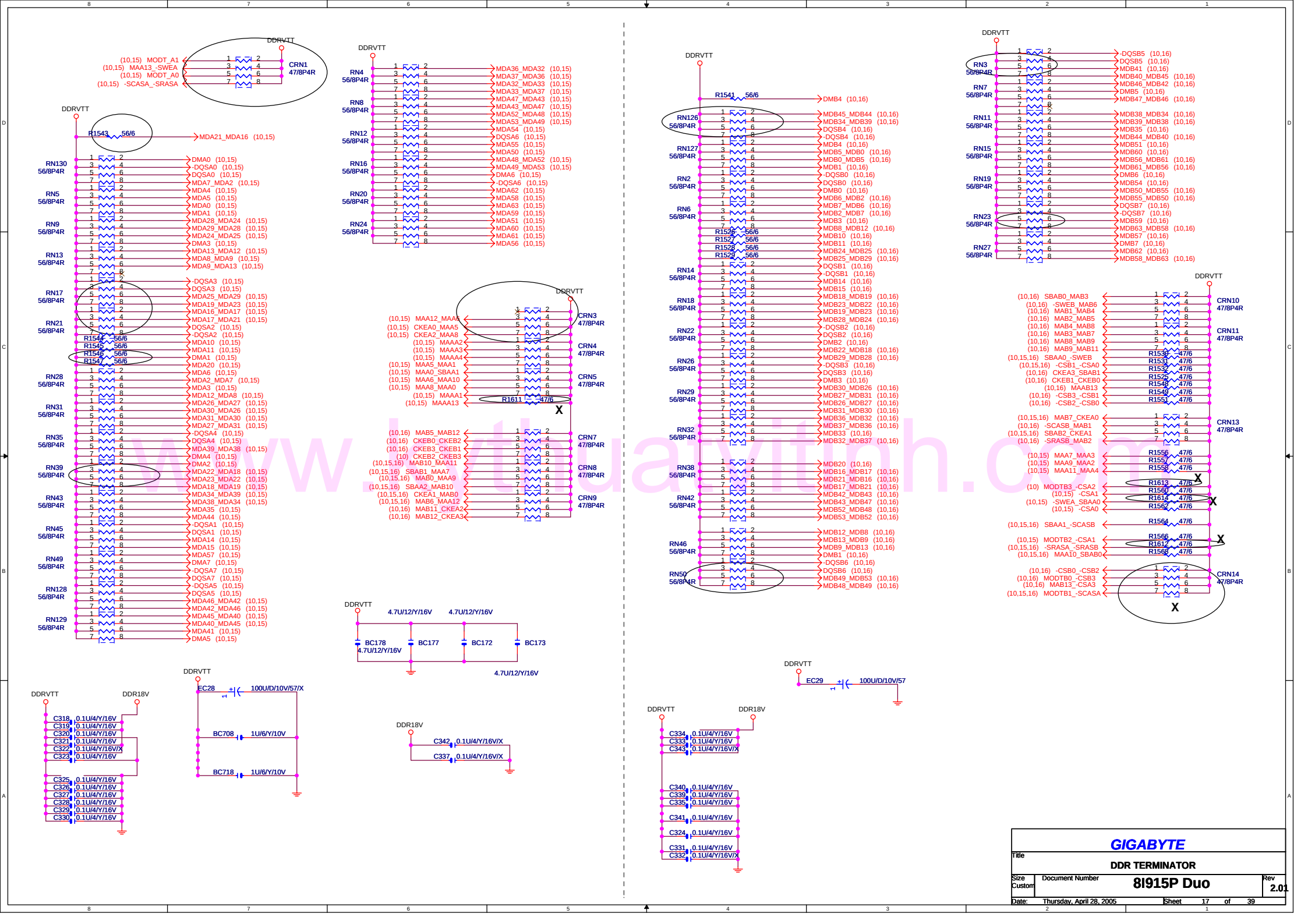
DDRVTT
CRN1 47/8P4R
(10,15) MODT_A1
(10,15) MAA13_-SWEA
(10,15) MODT_A0
(10,15) -SCASA_-SRASA
R1543 56/6
MDA21_MDA16 (10,15)
RN130 56/8P4R
RN5 56/8P4R
RN9 56/8P4R
RN13 56/8P4R
RN17 56/8P4R
RN21 56/8P4R
RN28 56/8P4R
RN31 56/8P4R
RN35 56/8P4R
RN39 56/8P4R
RN43 56/8P4R
RN45 56/8P4R
RN49 56/8P4R
RN128 56/8P4R
RN129 56/8P4R
R1544 56/6
R1545 56/6
R1546 56/6
R1547 56/6
RN4 56/8P4R
RN8 56/8P4R
RN12 56/8P4R
RN16 56/8P4R
RN20 56/8P4R
RN24 56/8P4R
CRN3 47/8P4R
CRN4 47/8P4R
CRN5 47/8P4R
CRN7 47/8P4R
CRN8 47/8P4R
CRN9 47/8P4R
R1611 47/6
X
DDR18V
C318 0.1U/4/Y/16V
C319 0.1U/4/Y/16V
C320 0.1U/4/Y/16V
C321 0.1U/4/Y/16V
C322 0.1U/4/Y/16V/X
C323 0.1U/4/Y/16V
C325 0.1U/4/Y/16V
C326 0.1U/4/Y/16V
C327 0.1U/4/Y/16V
C328 0.1U/4/Y/16V
C329 0.1U/4/Y/16V
C330 0.1U/4/Y/16V
EC28 100U/D/10V/57/X
BC708 1U/6/Y/10V
BC718 1U/6/Y/10V
4.7U/12/Y/16V
BC178 4.7U/12/Y/16V
BC177
BC172
BC173
C342 0.1U/4/Y/16V/X
C337 0.1U/4/Y/16V/X
R1541 56/6
RN126 56/8P4R
RN127 56/8P4R
RN2 56/8P4R
RN6 56/8P4R
R1526 56/6
R1527 56/6
R1528 56/6
R1529 56/6
RN14 56/8P4R
RN18 56/8P4R
RN22 56/8P4R
RN26 56/8P4R
RN29 56/8P4R
RN32 56/8P4R
RN38 56/8P4R
RN42 56/8P4R
RN46 56/8P4R
RN50 56/8P4R
EC29 100U/D/10V/57
C334 0.1U/4/Y/16V
C333 0.1U/4/Y/16V
C343 0.1U/4/Y/16V/X
C340 0.1U/4/Y/16V
C339 0.1U/4/Y/16V
C335 0.1U/4/Y/16V
C341 0.1U/4/Y/16V
C324 0.1U/4/Y/16V
C331 0.1U/4/Y/16V
C332 0.1U/4/Y/16V/X
RN3 56/8P4R
RN7 56/8P4R
RN11 56/8P4R
RN15 56/8P4R
RN19 56/8P4R
RN23 56/8P4R
RN27 56/8P4R
CRN10 47/8P4R
CRN11 47/8P4R
CRN13 47/8P4R
CRN14 47/8P4R
R1530 47/6
R1531 47/6
R1532 47/6
R1525 47/6
R1548 47/6
R1549 47/6
R1552 47/6
R1556 47/6
R1557 47/6
R1558 47/6
R1613 47/6
R1560 47/6
R1614 47/6
R1562 47/6
R1564 47/6
R1566 47/6
R1612 47/6
R1568 47/6
X
GIGABYTE
Title
DDR TERMINATOR
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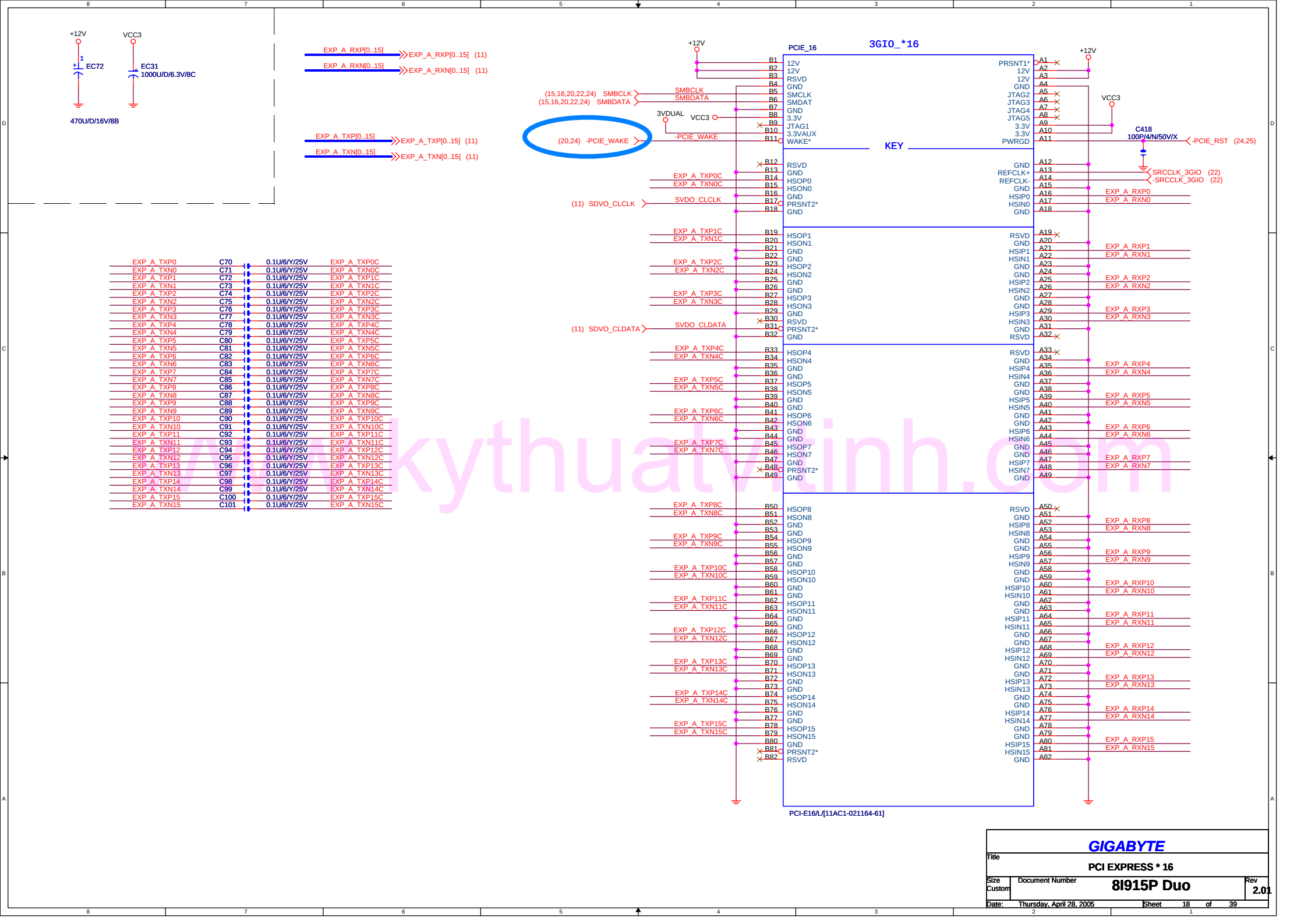

Title	PCI EXPRESS * 16
Size	Custom
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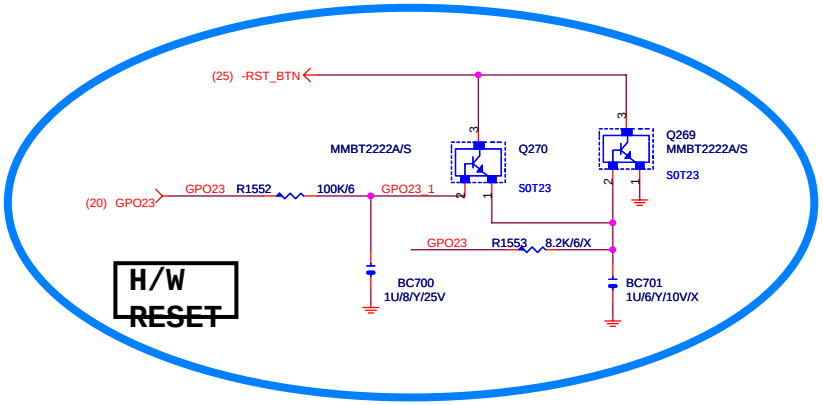
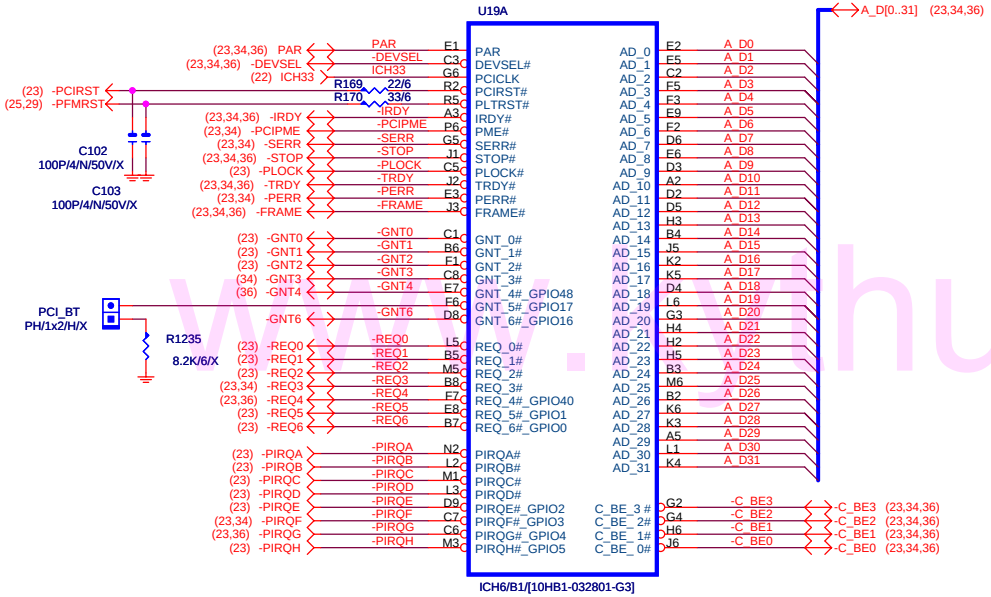
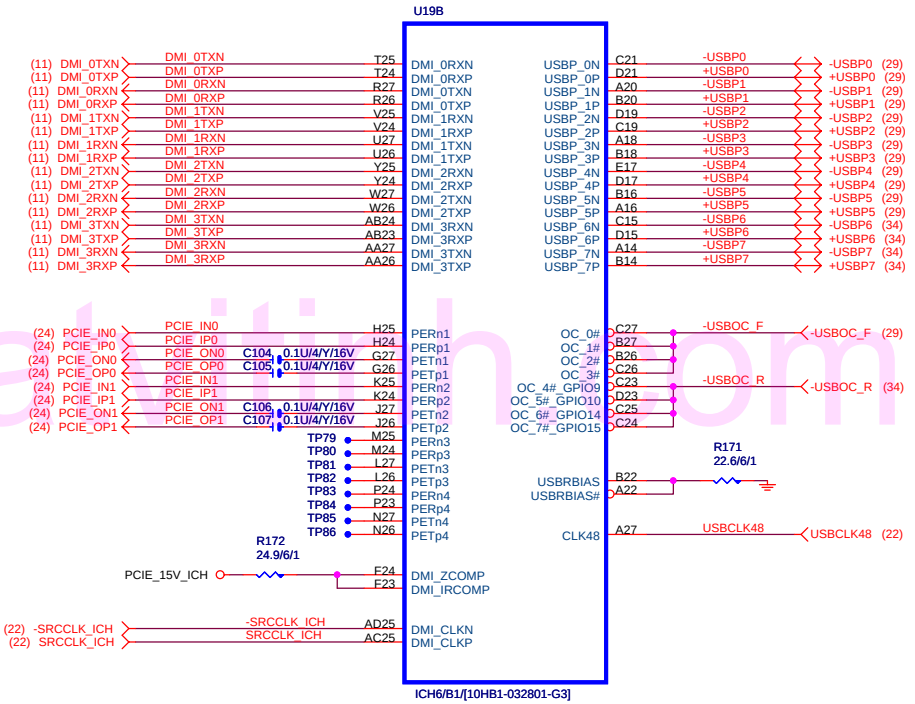
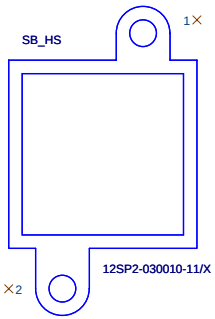


DMI Connection Note
GMCH TX Pin Need Connect to ICH6 RX Pin
ICH6 TX Pin Need Connect to GMCH RX Pin







GIGABYTE			
Title	ICH6-PCI, DMI, LAN, USB		
Size B	Document Number 8I915P Duo		Rev 2.01
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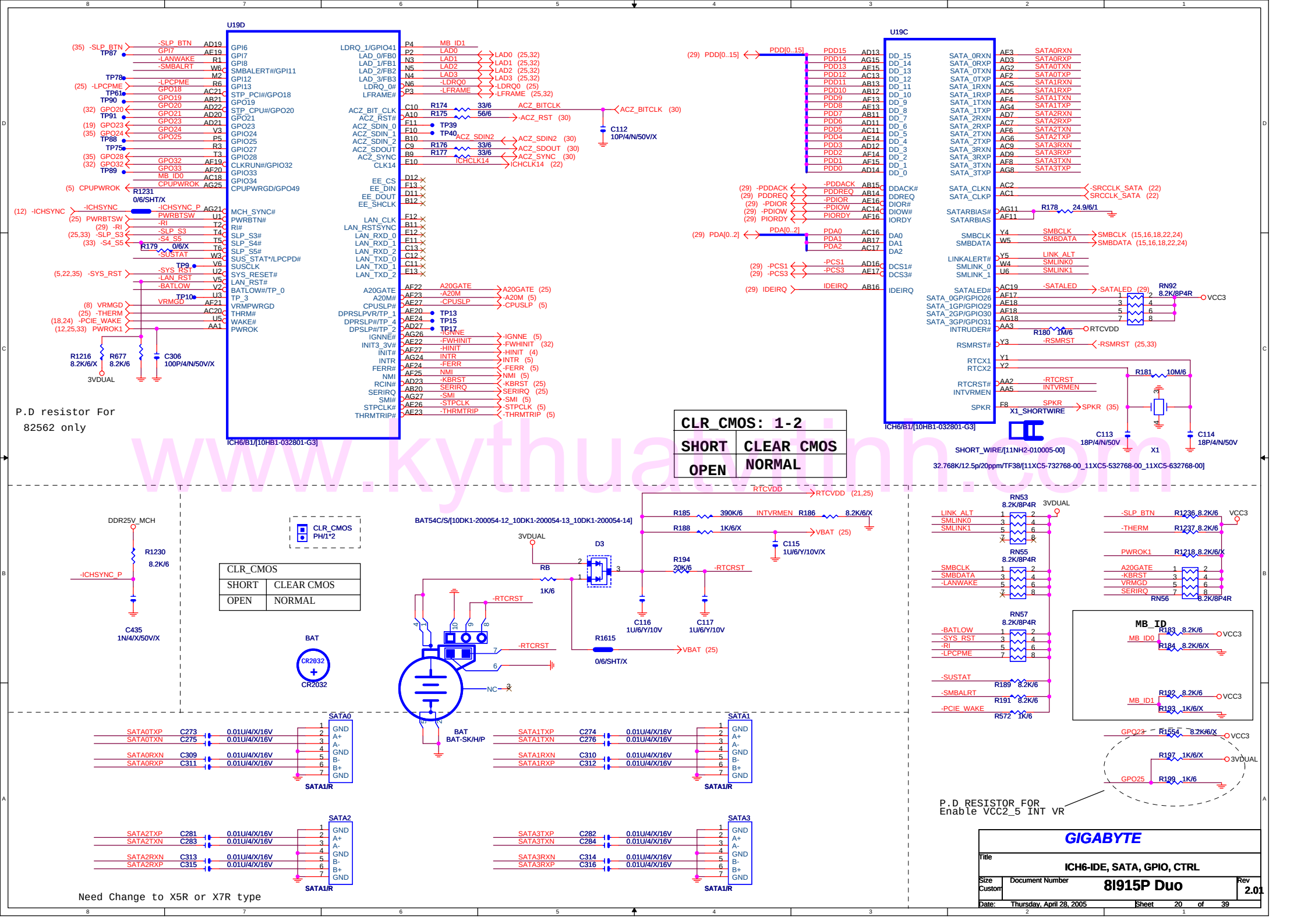

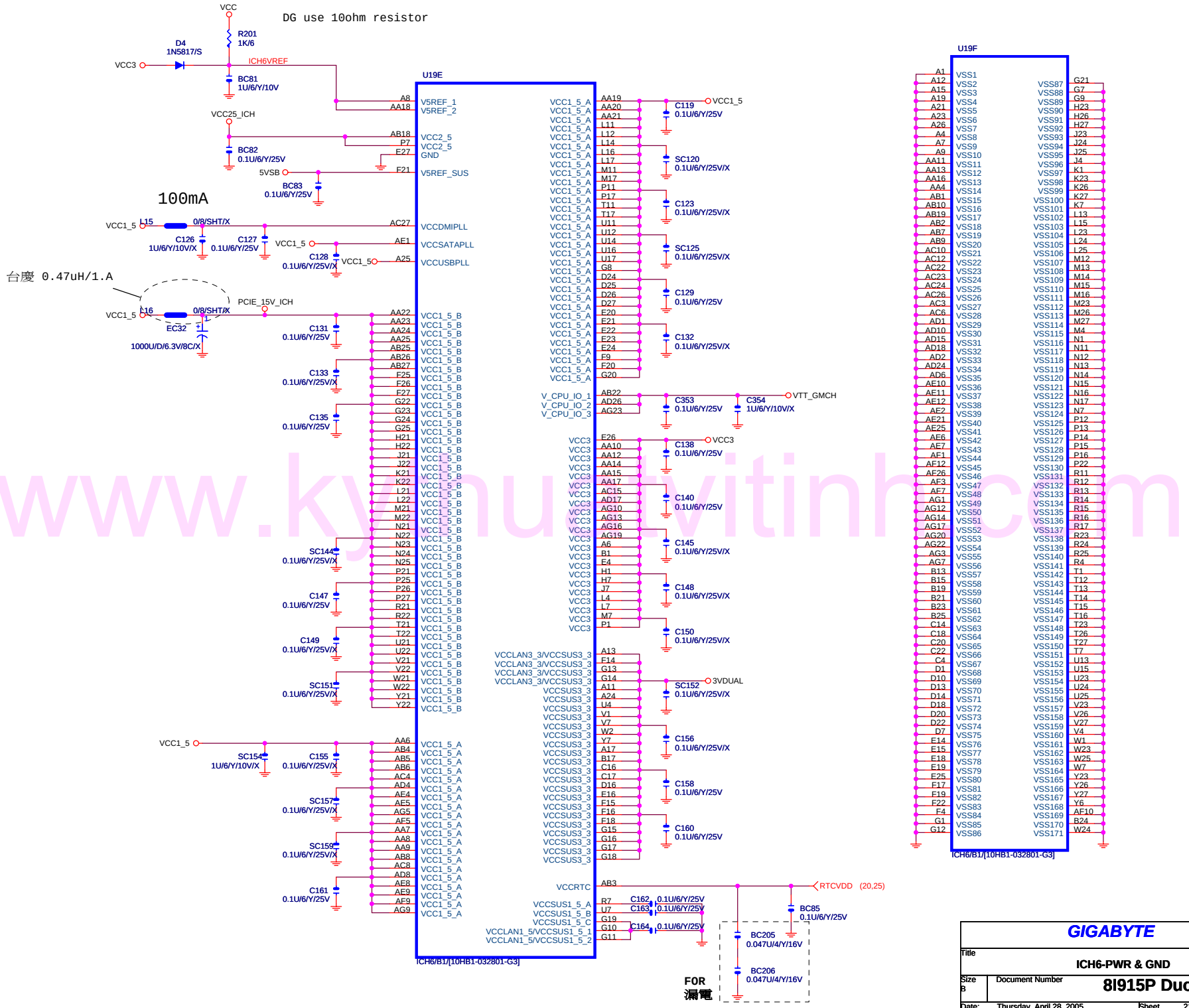

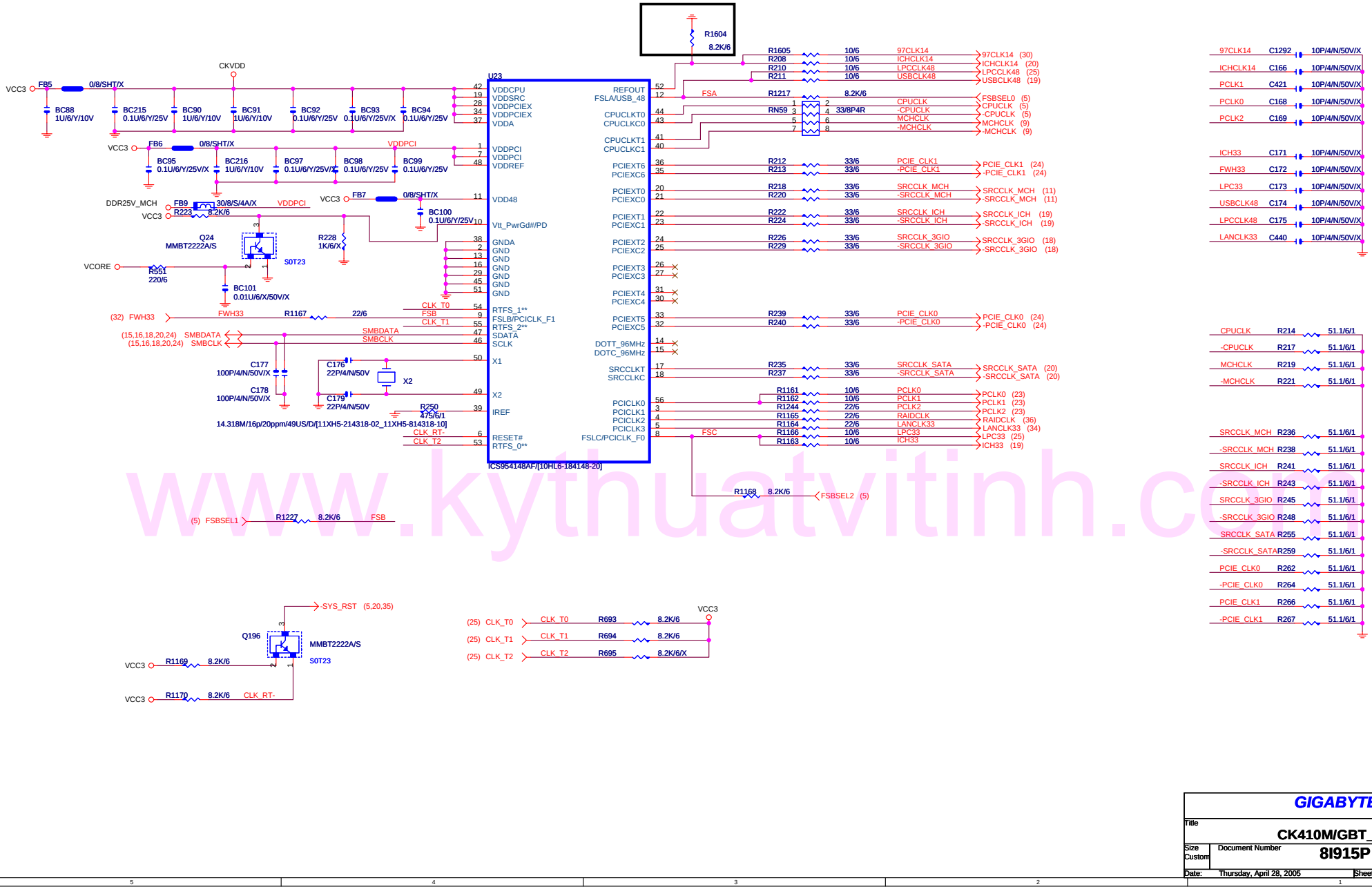

GIGABYTE

Title	CK410M/GBT_CLK GEN	
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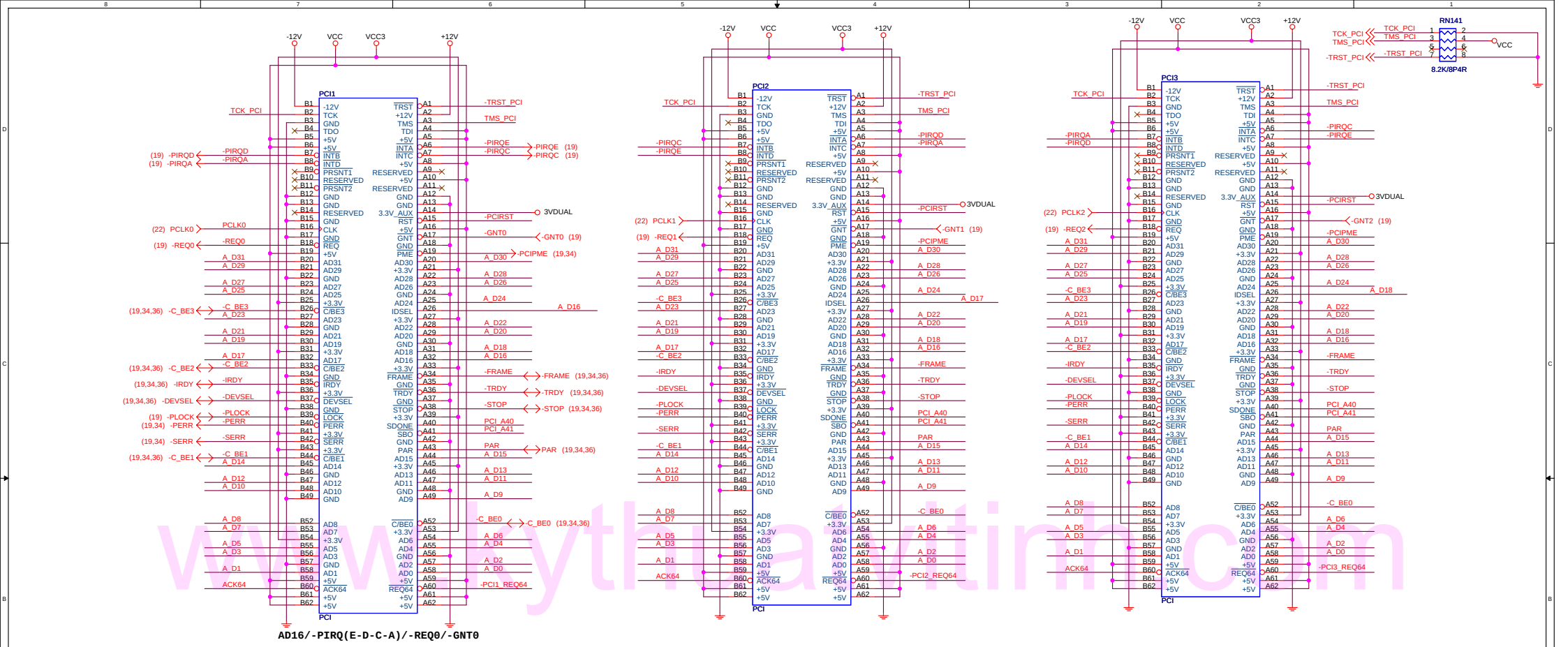
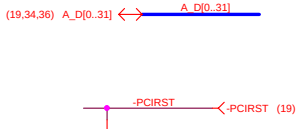
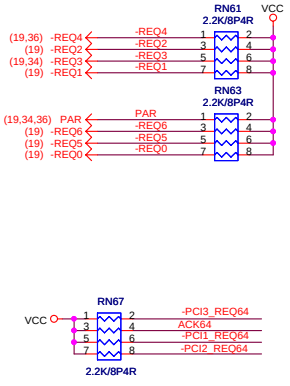
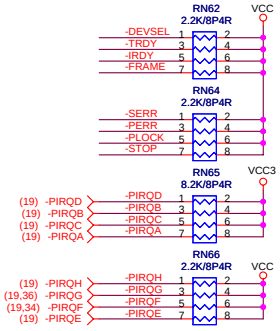
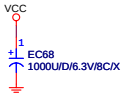




Place close to PCI1







GIGABYTE			
Title: PCI SLOT			
Size: Custom	Document Number: 8I915P Duo		Rev: 2.01
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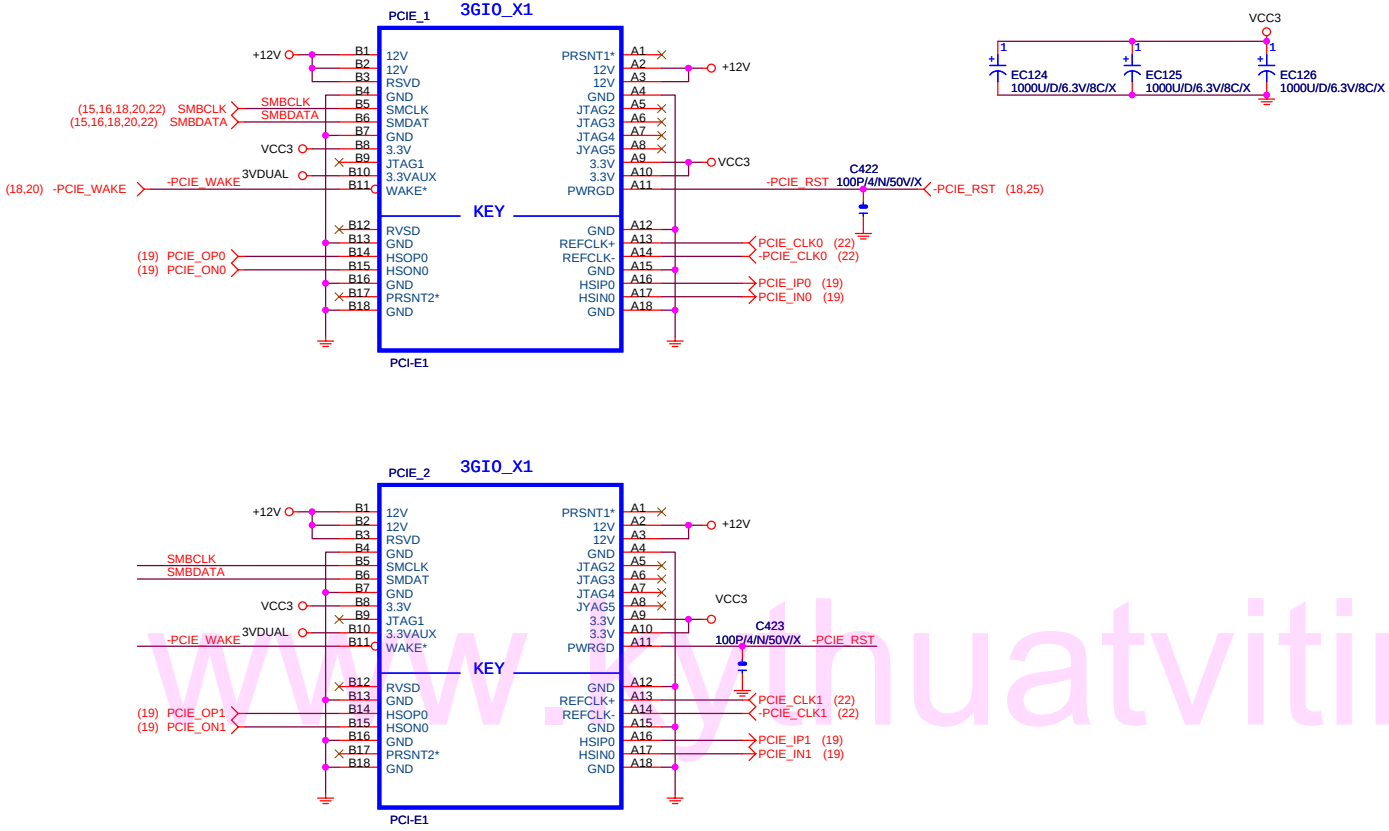

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Title	PCI E SLOT	
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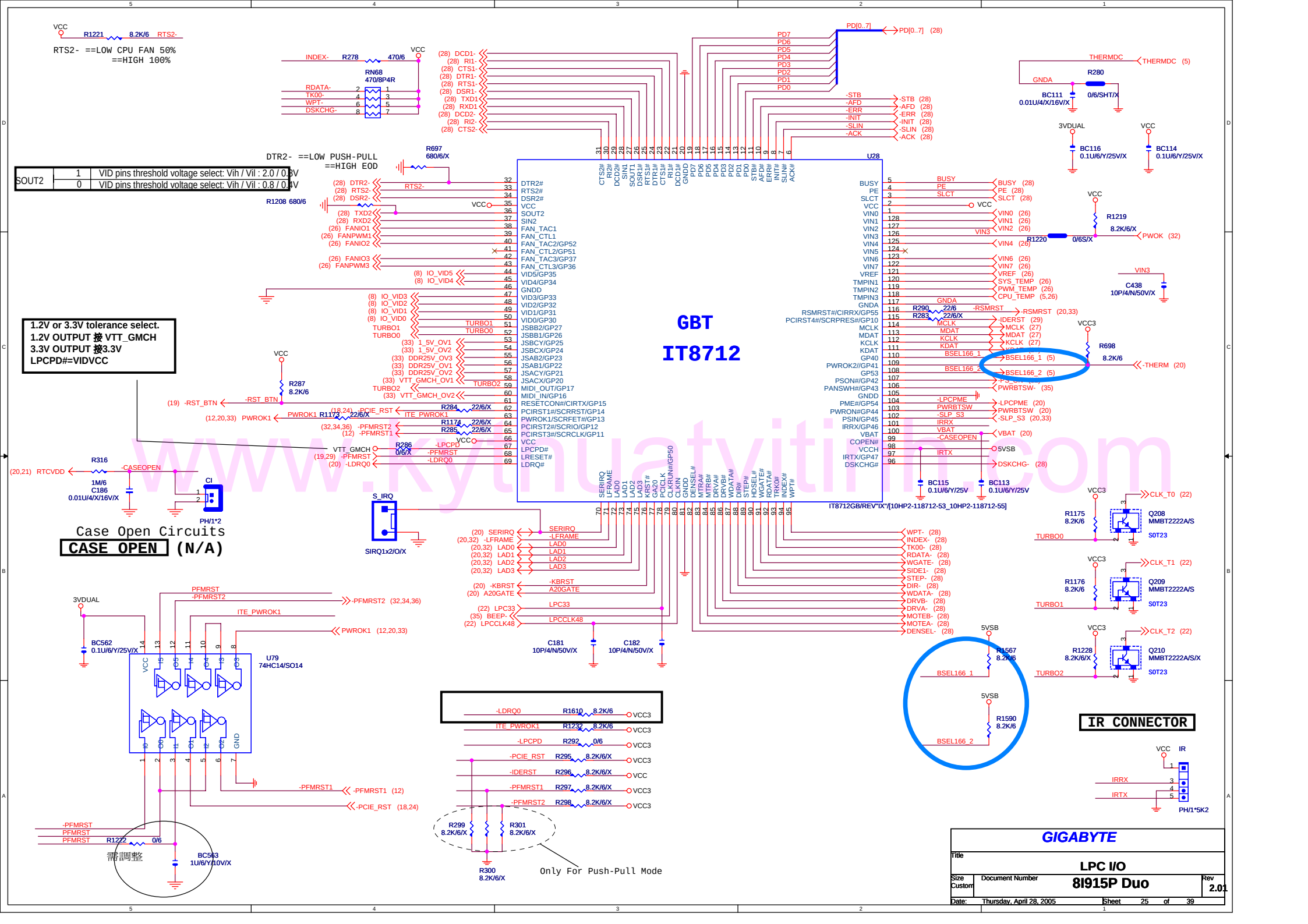
RTS2- ==LOW CPU FAN 50%
==HIGH 100%
DTR2- ==LOW PUSH-PULL
==HIGH EOD
SOUT2
1 VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
0 VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V
1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接3.3V
LPCPD#=VIDVCC
GBT
IT8712
IT8712GB/REV"IX"/[10HP2-118712-53_10HP2-118712-55]
Case Open Circuits
CASE OPEN (N/A)
IR CONNECTOR
需調整
Only For Push-Pull Mode
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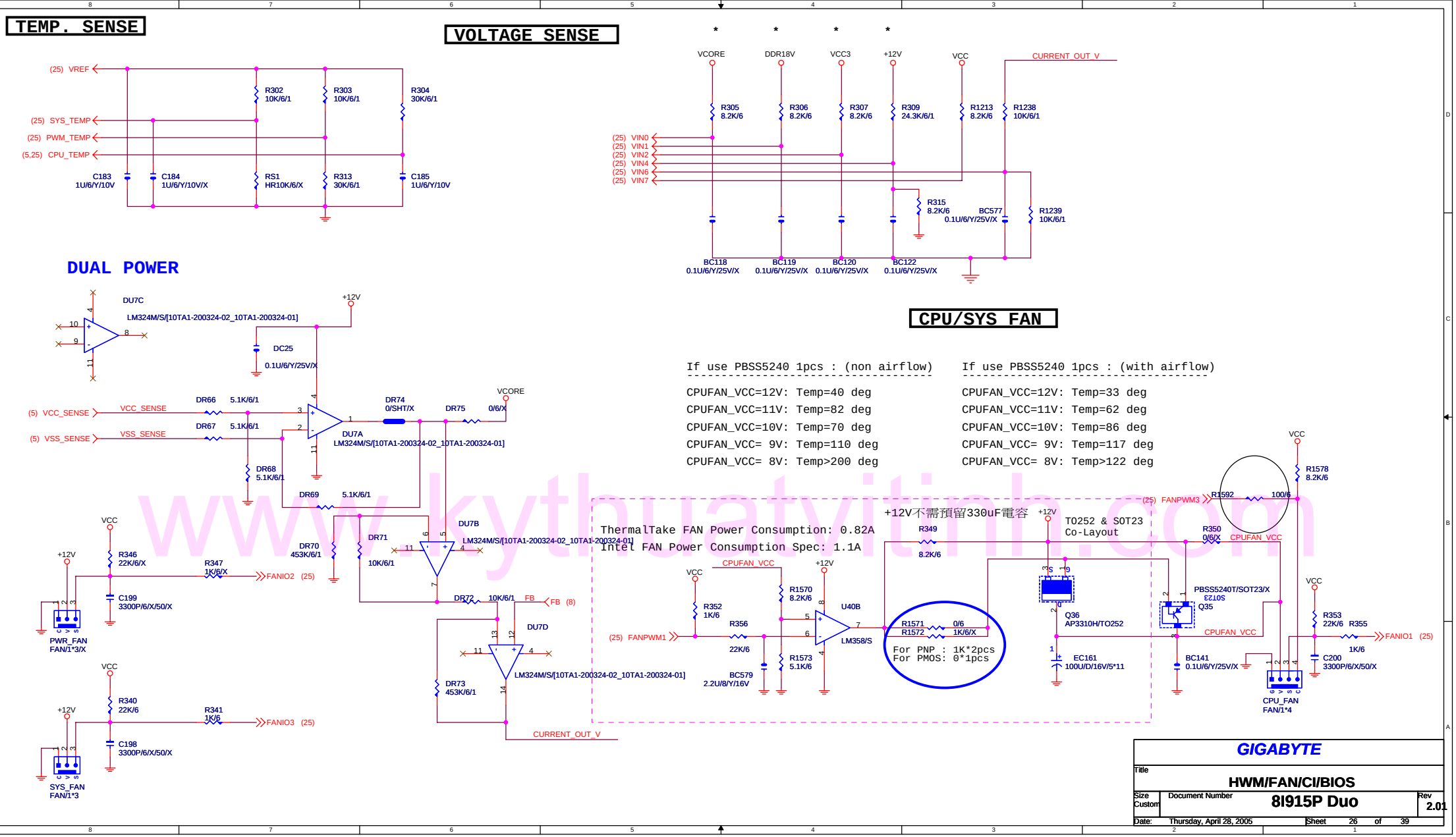
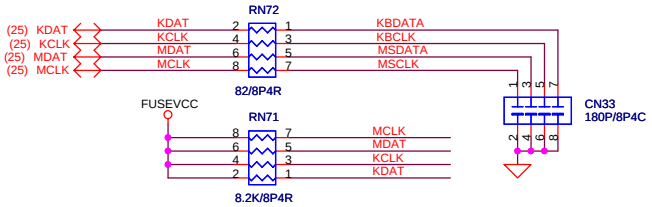
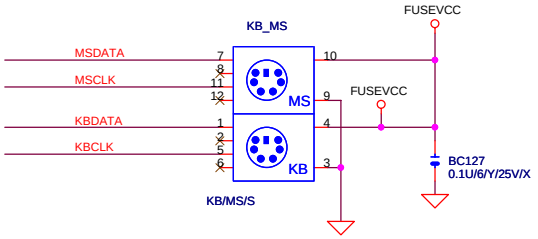
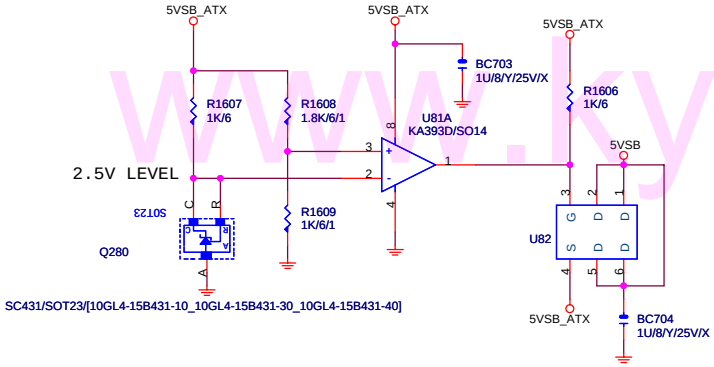


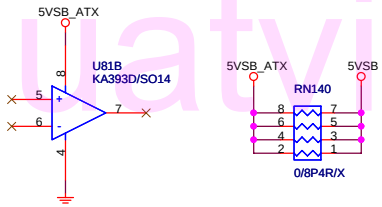
KB/MS

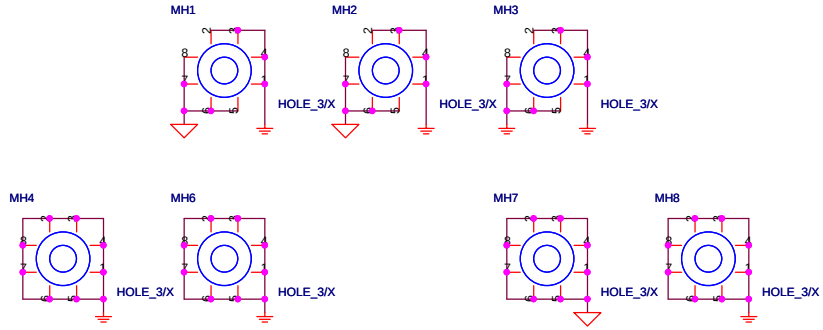


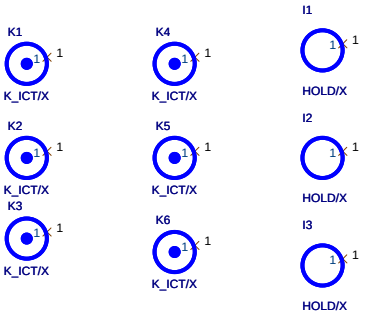


S.P.P.









GIGABYTE

Title	PS/2 KB & MS	
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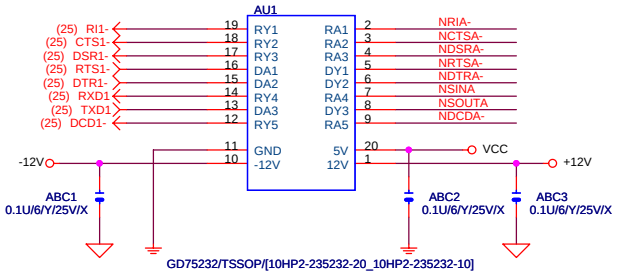
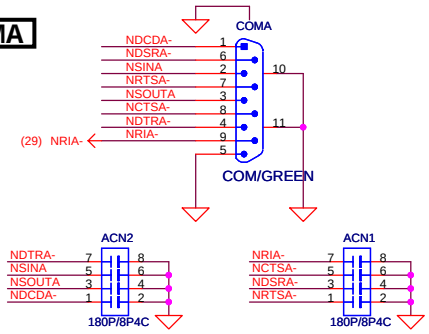
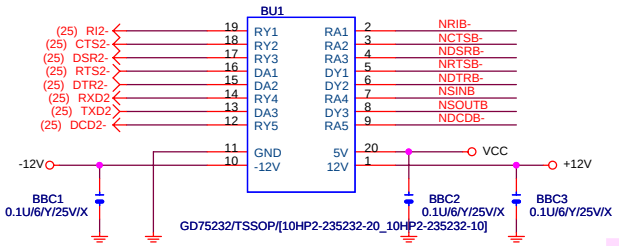
COMA/COMB



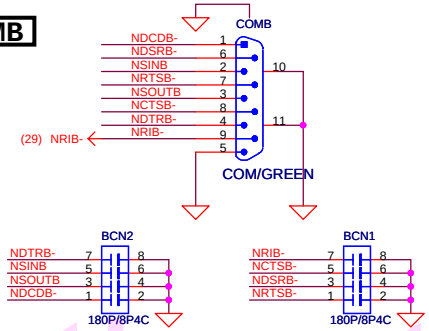
COMA



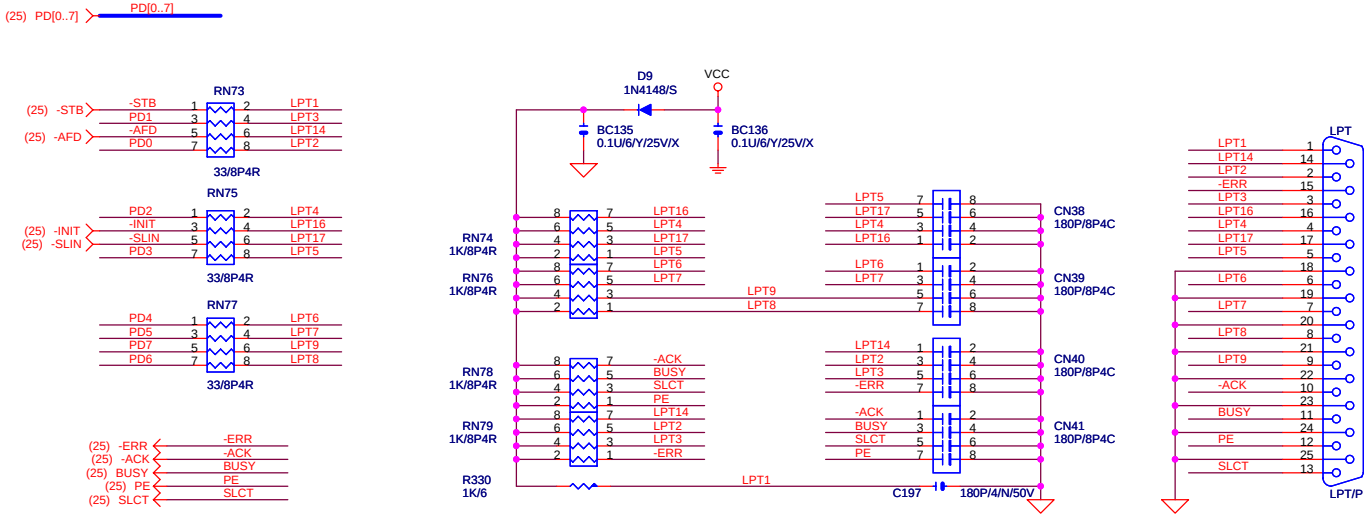
COMB



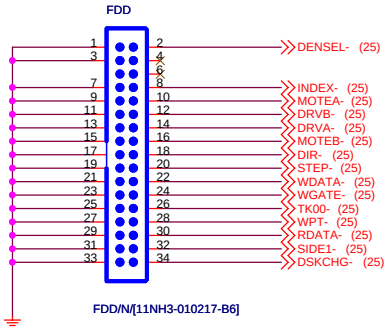
COMB



LPT



FLOPPY



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Title	COM, LPT, FDD	
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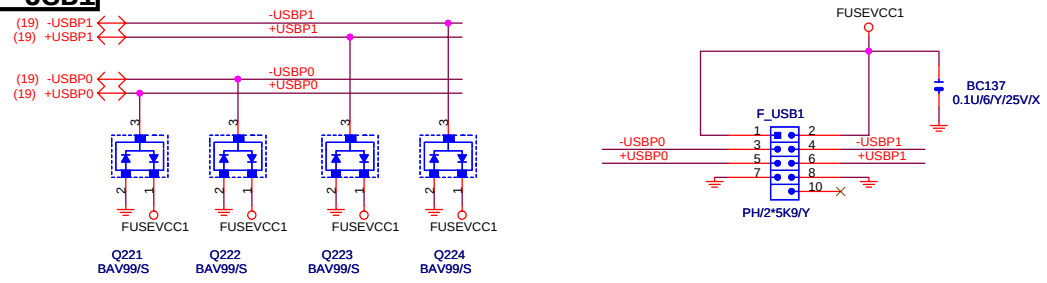
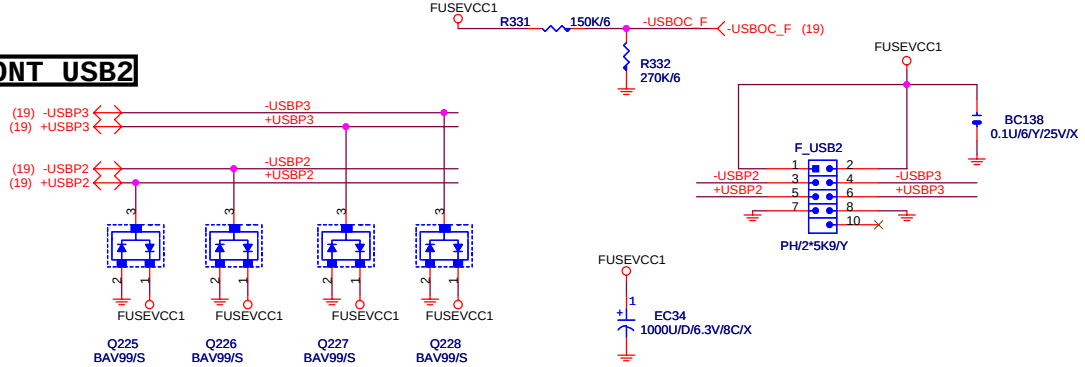
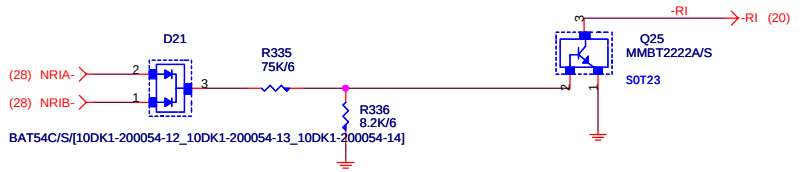
FRONT USB1



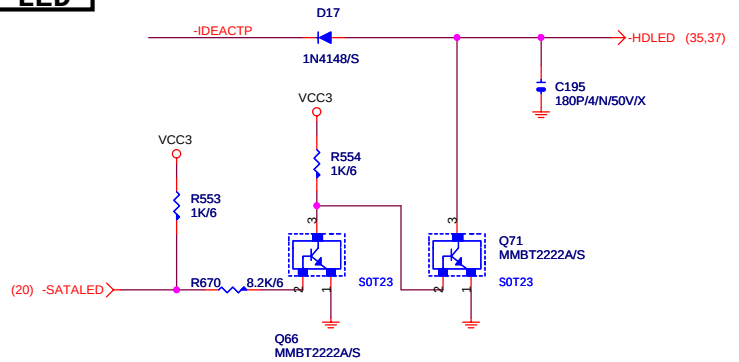
FRONT USB2



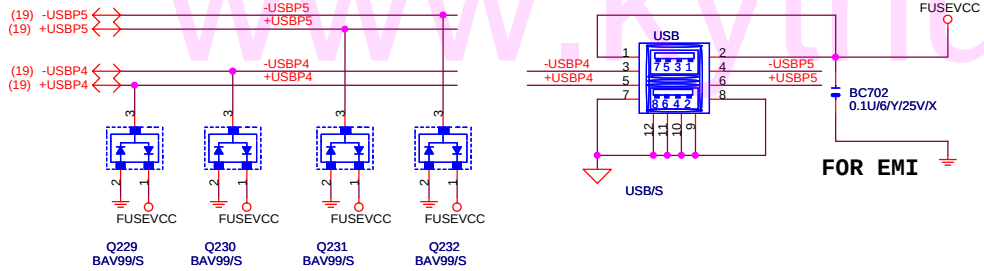
RING IN



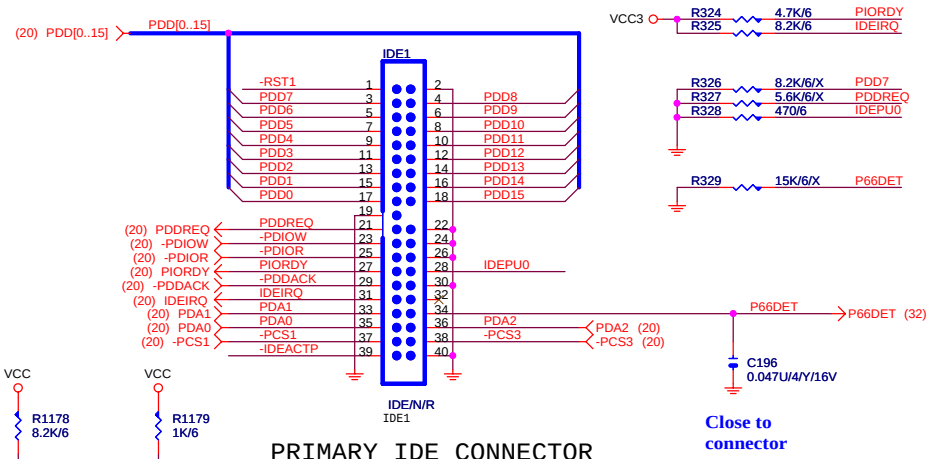
IDE/SATA LED



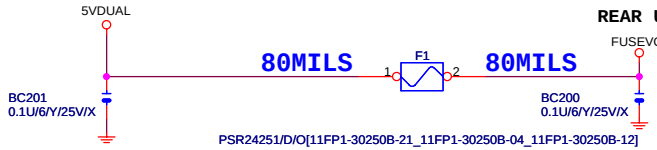
FUSEVCC, GAMEVCC



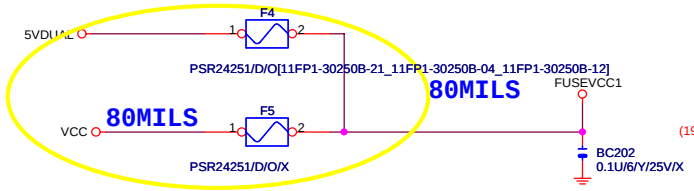
IDE



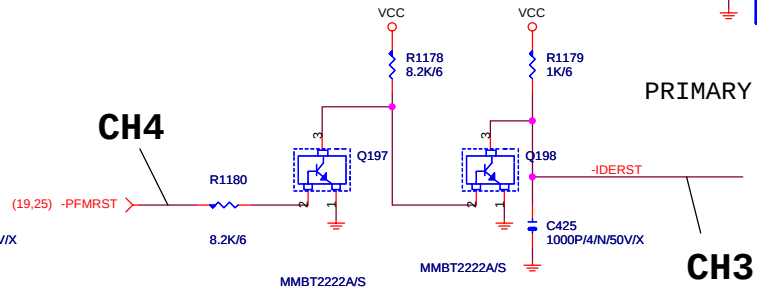
160MILS



FRONT USB



CH4



GIGABYTE		
Title	FRONT/REAR USB CONNECTOR/IDE	
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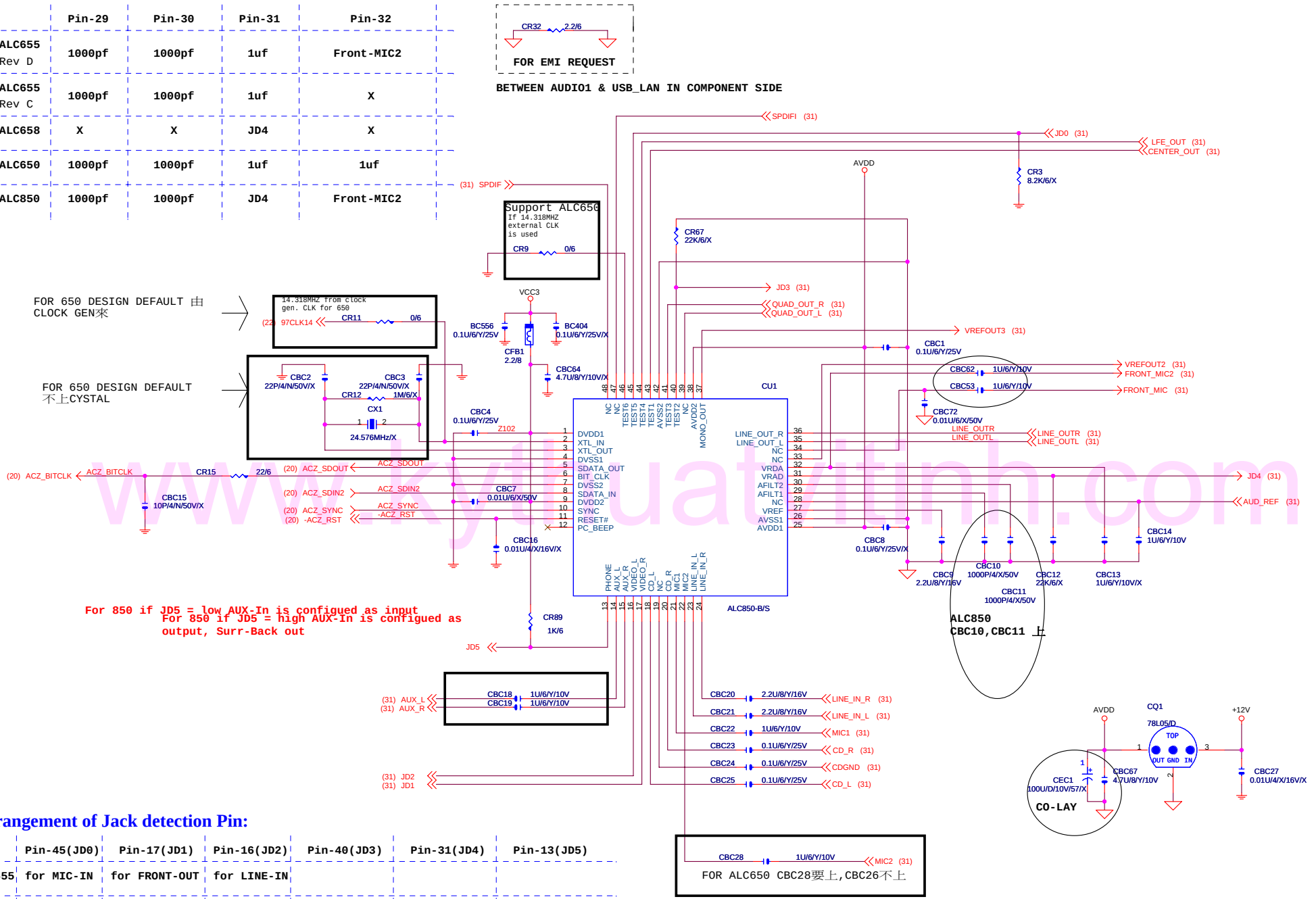
Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2



Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT Exernal pull high is needed	for LINE-IN Exernal pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

For 850 if JD5 = low AUX-In is configued as input
For 850 if JD5 = high AUX-In is configued as output, Surr-Back out

GIGABYTE CORP.	
Title	ALC850
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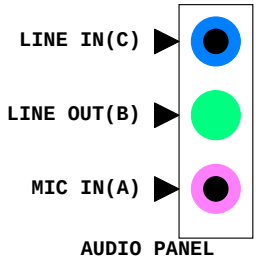
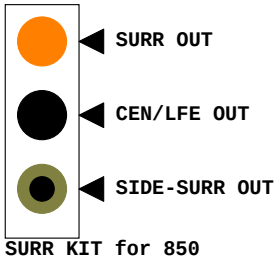
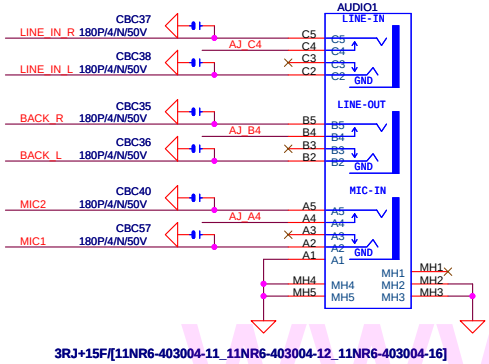


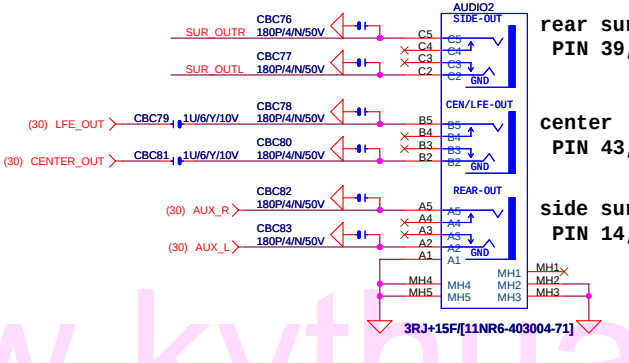
AUDIO PANEL
AUDIO1



SURR KIT for 850
AUDIO2



3RJ+15F/[11NR6-403004-11_11NR6-403004-12_11NR6-403004-16]

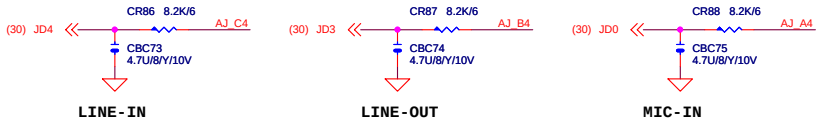


3RJ+15F/[11NR6-403004-71]

rear surround
PIN 39,41

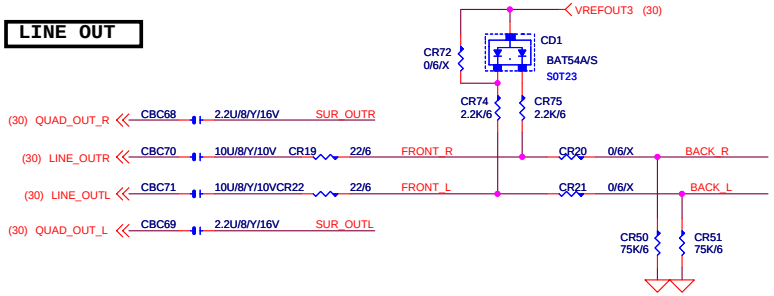
center
PIN 43,44

side surround
PIN 14,15

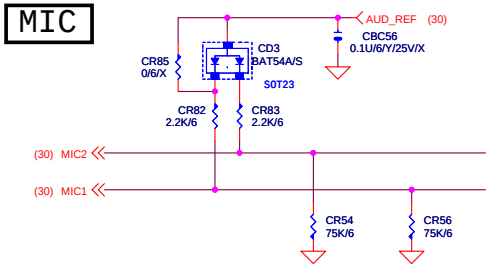


LINE-IN LINE-OUT MIC-IN

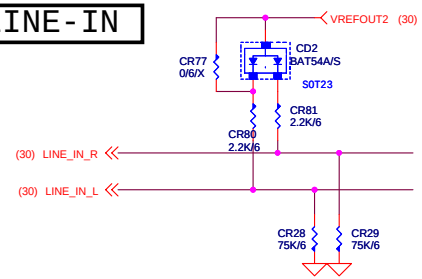
LINE OUT



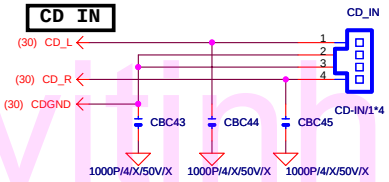
MIC



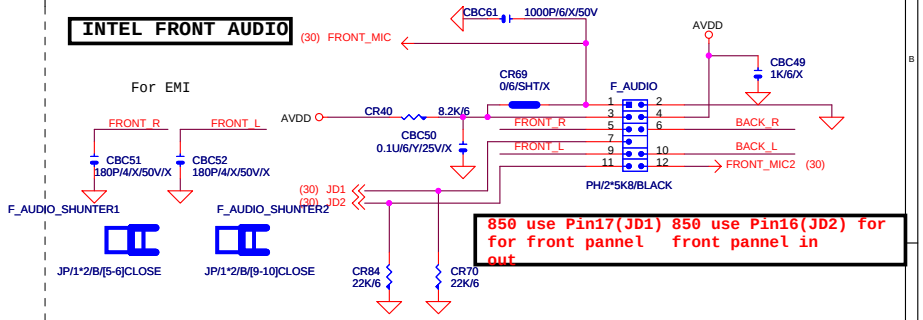
LINE-IN



CD IN

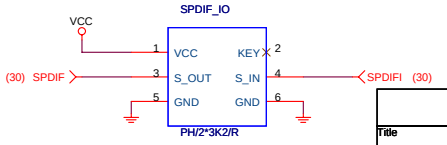


INTEL FRONT AUDIO



850 use Pin17(JD1) 850 use Pin16(JD2) for for front pannel front pannel in out

SPDIF_IO



GIGABYTE CORP.

Title: AUDIO OUTPUT,GAME PORT

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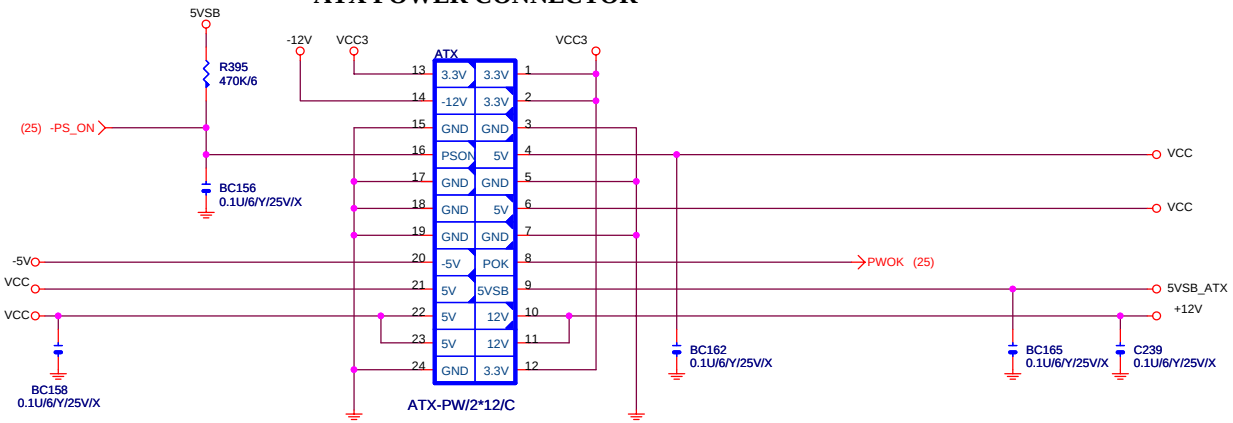
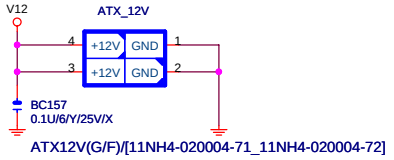
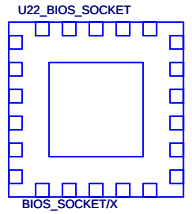
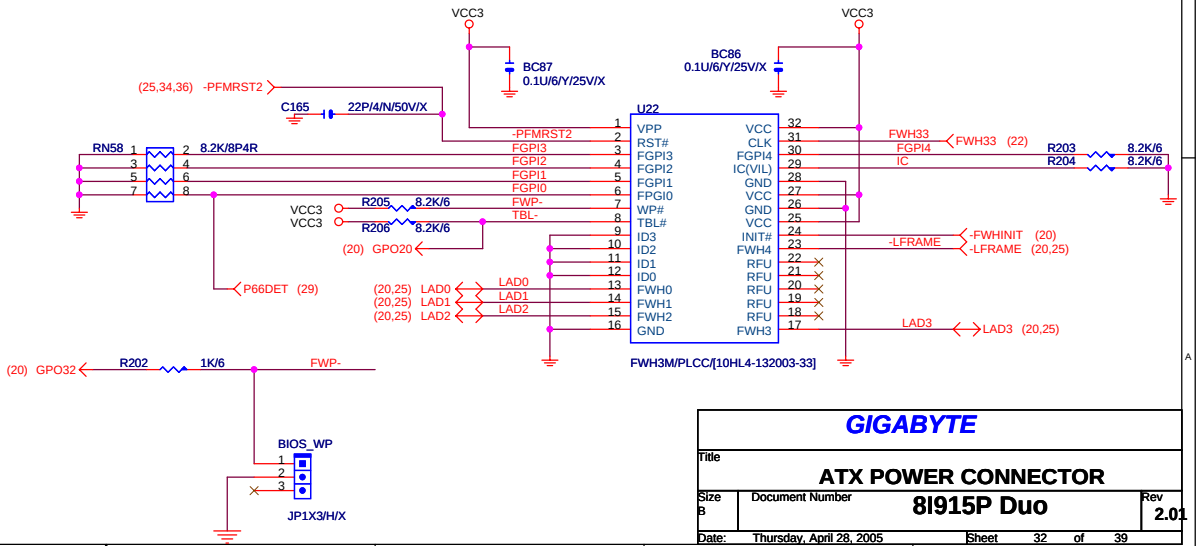
ATX POWER CONNECTOR







FWH BIOS



GIGABYTE		
Title: ATX POWER CONNECTOR		
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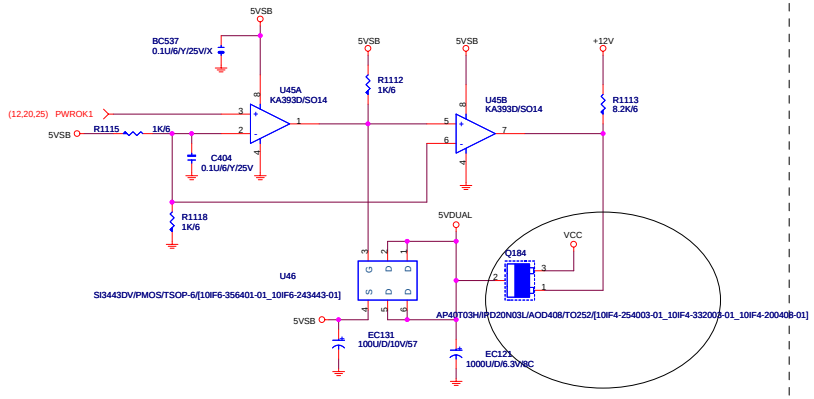
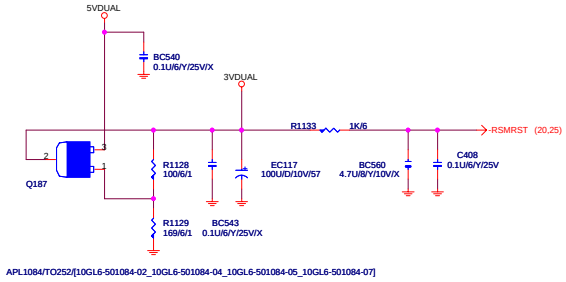
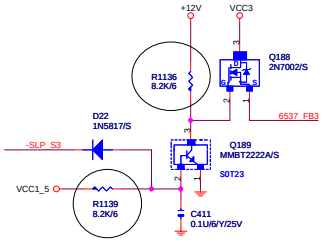
5VDUAL CIRCUIT

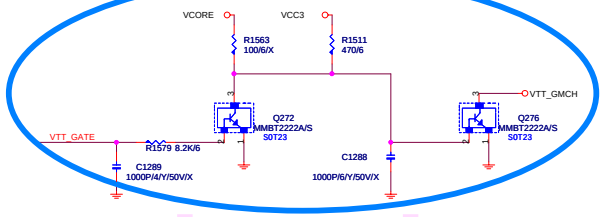


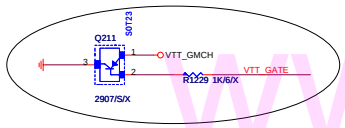
3VDUAL CIRCUIT

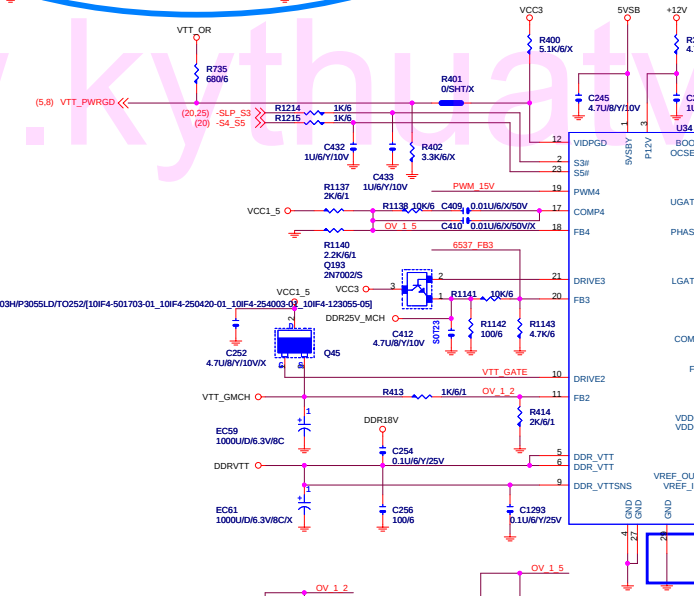


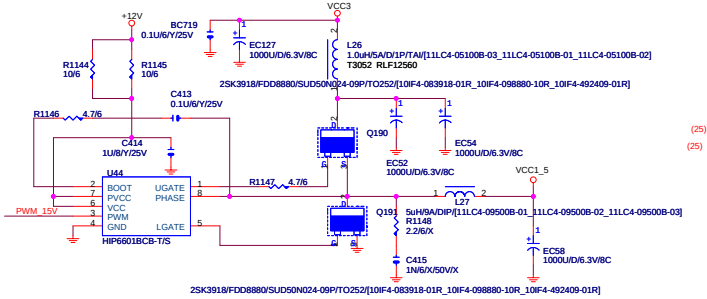
DDR25V/VCC1_5/VTT_GMCH/DDRVTT











GIGABYTE			
Title: Discrete Power			
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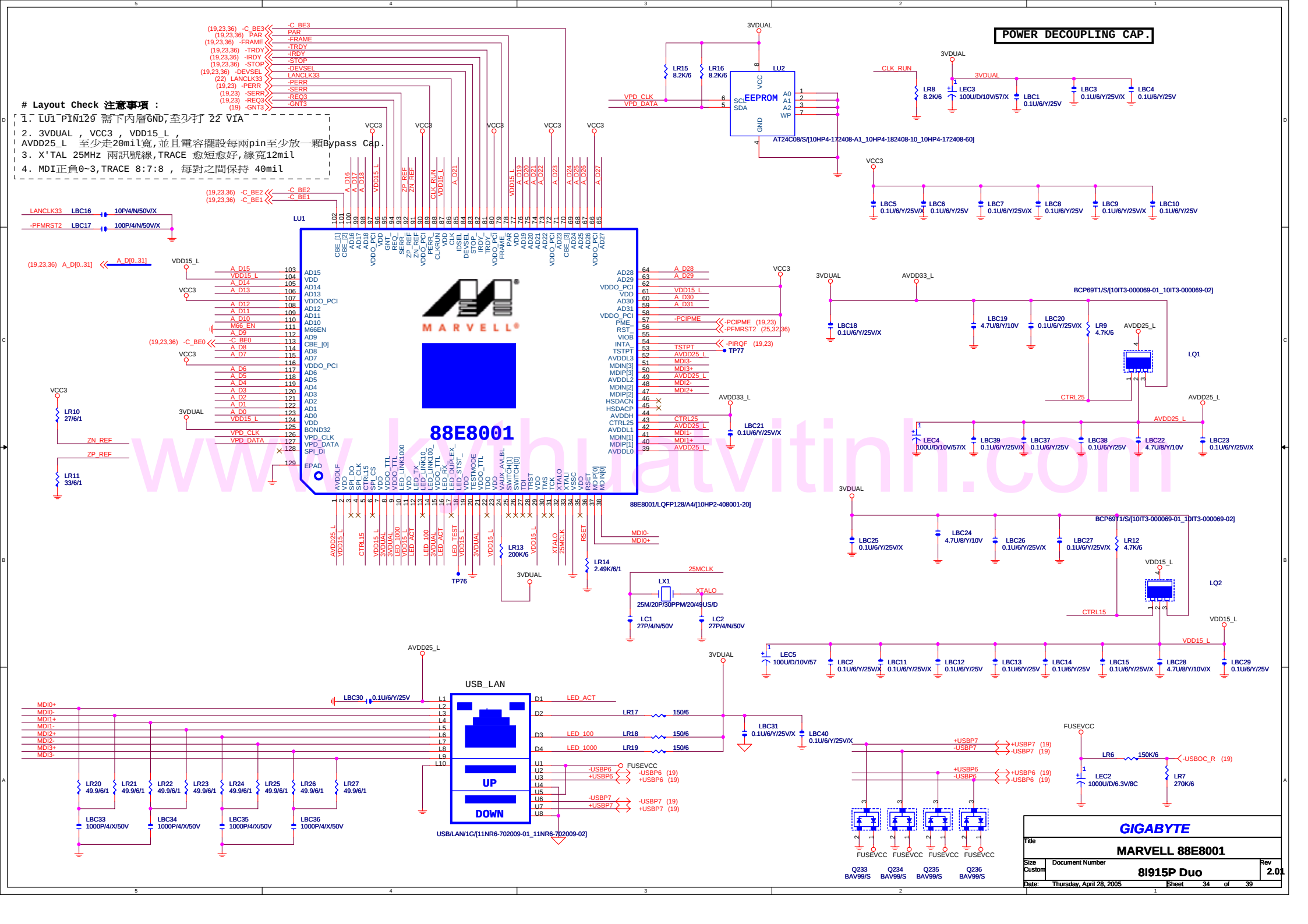
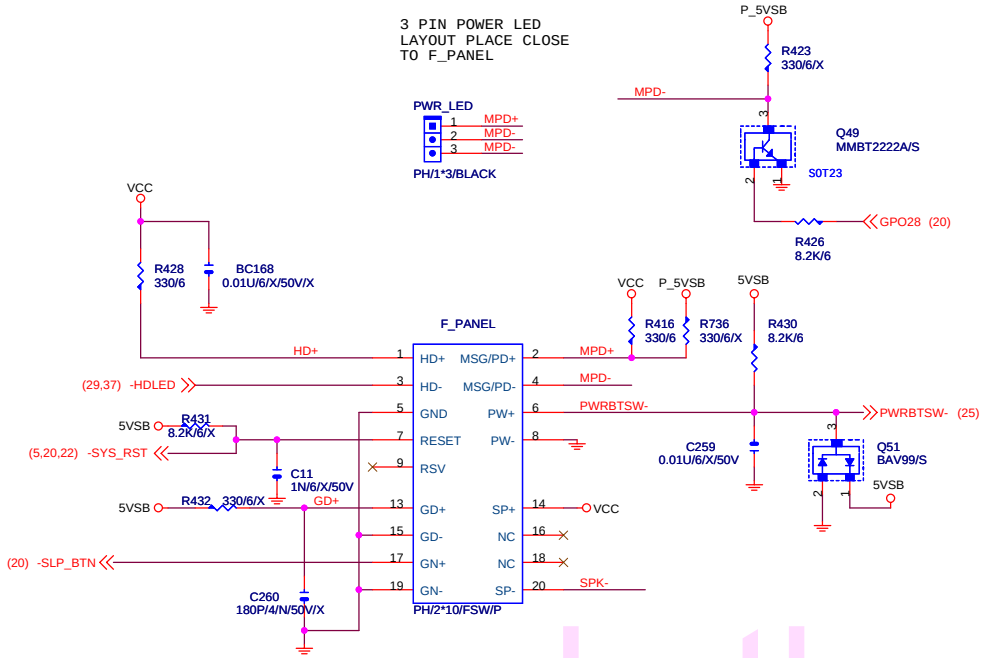


INTEL FRONT PANEL



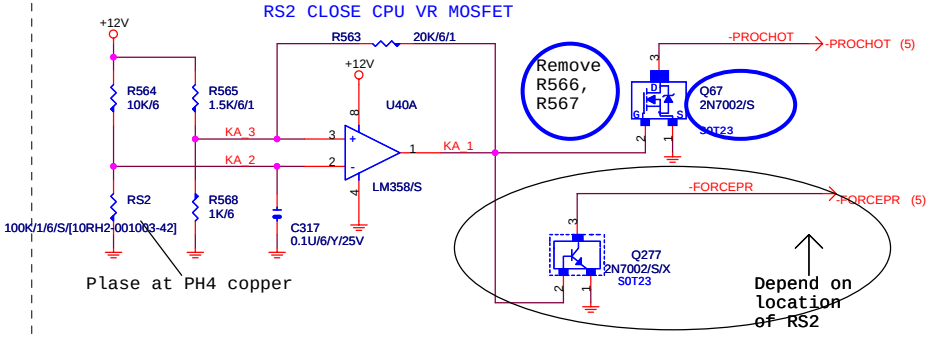
PROCESSOR HOT (N/A)

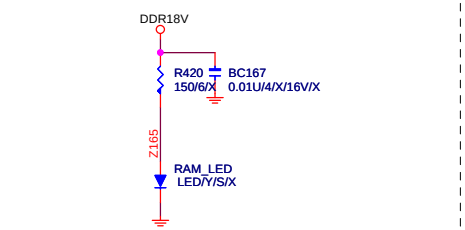
如果要用2N7002需注意OP output
Hi時的電壓是否遠大於2V。

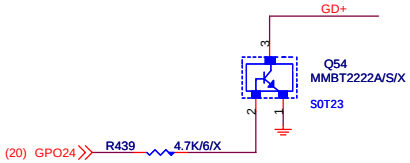
asserted at 130 degree (RS2=720 ohm)
deasserted at 115 degree (RS2=1270 ohm)

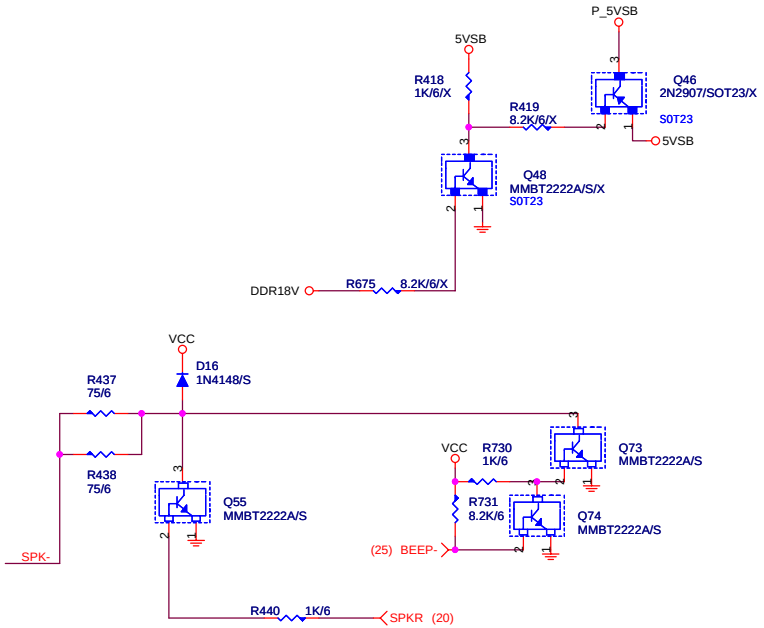
KA393改爲LM358，電源pin改接+12V，Prochot#溫度需重新調整之。

RS2 CLOSE CPU VR MOSFET









States for green LED NO1 GPO22 only S1 PROGRAMMING LOW

LED States	ACPI States	GPO28
ON	S1,S3	0
OFF	S0,S5	1

(GPO22 DEFAULT HIGH, main power)

States for a single-color power LED

LED States	ACPI States	GPO25	GPO27	GPO24
OFF	S1,S3,S5	1	1	NO1
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1

LED States	ACPI States	GPO25	GPO27	GPO22
OFF	S5	1	1	X
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1
Steady Yellow	S1,S3	1	0	NO1
Blinking Yellow	S1,S3(message waiting)	1	B	NO1

GIGABYTE

Title: FRONT PANEL

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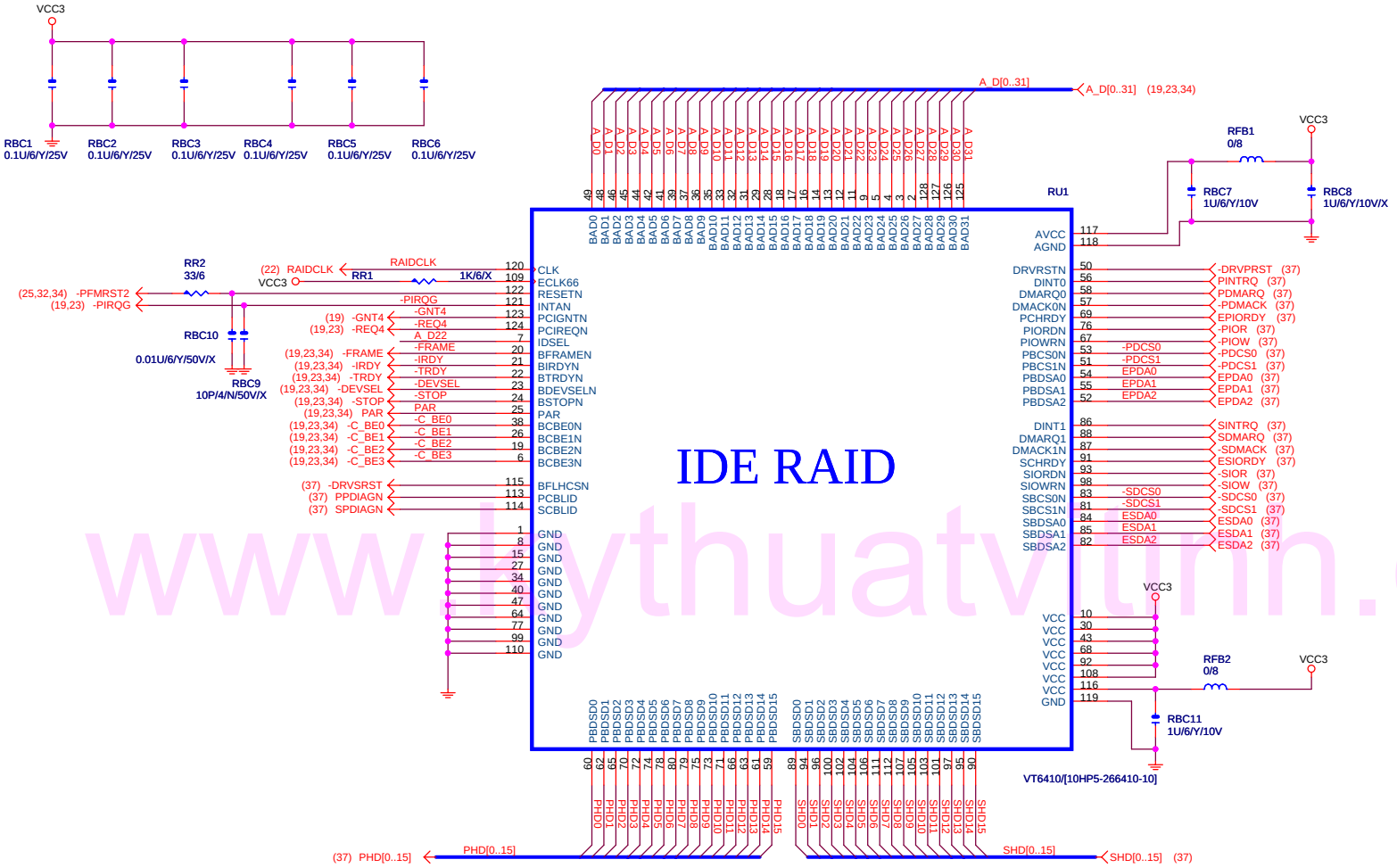
ALL INPUT PIN MUST HAVE 0.1 CAPACITOR



GIGABYTE		
Title	ATA100/133 & IDE RAID	
Size	Document Number: 8I915P Duo	Rev: 2.01
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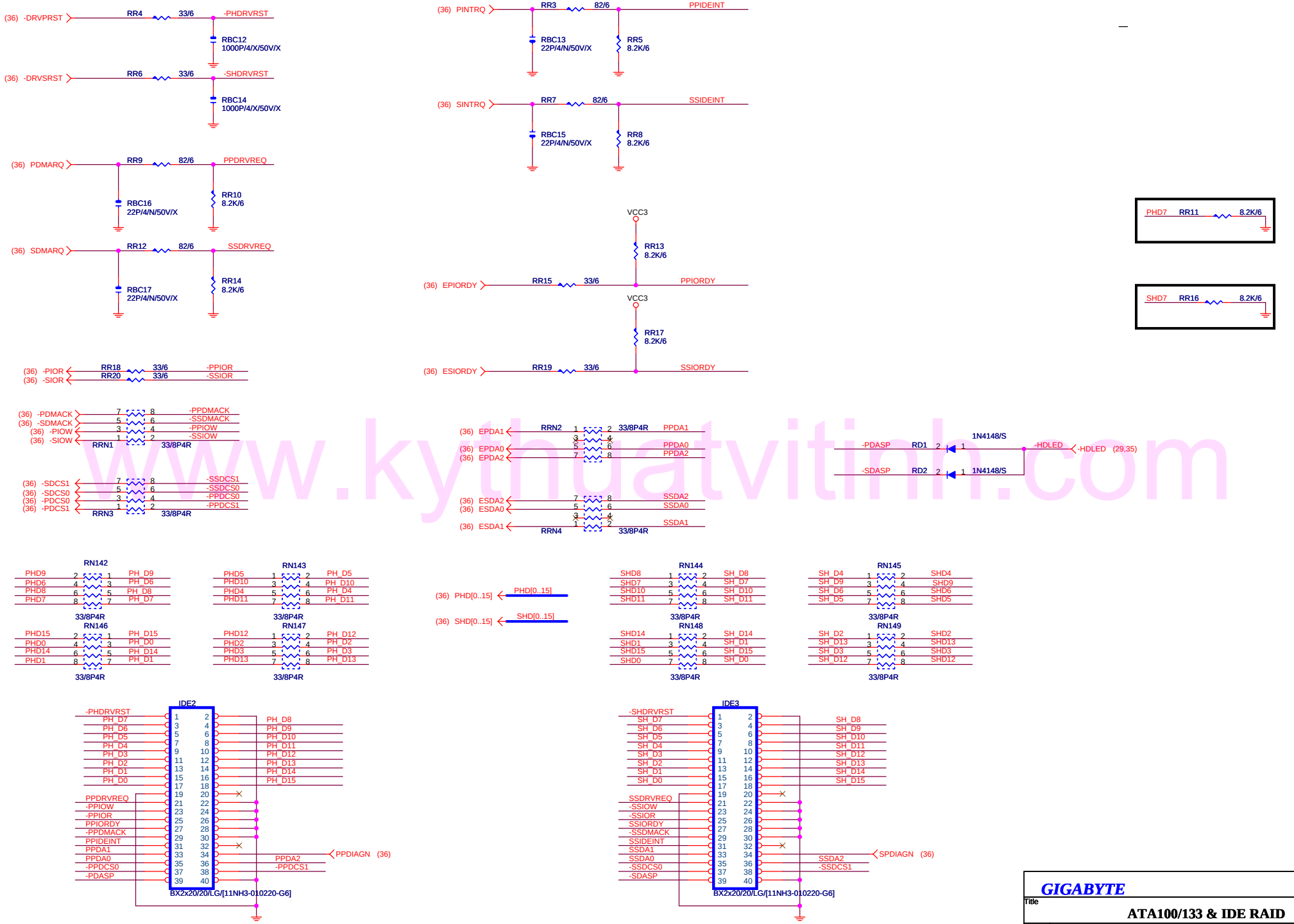

GIGABYTE

Title	ATA100/133 & IDE RAID	
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INTEL ICH6 GPIO Implementation

紅字表示CPI/O 同PIN

GPI PIN

Pin Name	Pin Type	Power Well			GPIO Application
GPI[0]	Input	V5REF	-REQ[6]	(P.U VCC)	-REQ[6]
GPI[1]	Input	V5REF	-REQ[5]	(P.U VCC)	Reserved
GPI[5:2]	Input	V5REF	-PIRQ[H:E]	(P.U VCC)	PCI/LAN/NA/1394
GPI[6]	Input	VCC3	GPI[6]	(P.U VCC3)	-SLP_BTN
GPI[7]	Input	VCC3	GPI[7]	(NA)	DUALBIOS_INPUT
GPI[8]	Input	3VDUAL	GPI[8]	(P.U 3VDUAL)	-LANWAKE
GPI[10:9]	Input	3VDUAL	0C_4/5	(P.U 5VDUAL分壓)	-USBOC_R
GPI[11]	Input	3VDUAL	-SMBALERT	(P.U 3VDUAL)	-SMBALRT
GPI[12]	Input	VCC3	GPI[12]	(P.U VCC3)	ATX24_DET
GPI[13]	Input	3VDUAL	GPI[13]	(P.U 3VDUAL)	-LPCPME
GPI[15:14]	Input	3VDUAL	0C_6/7	(P.U 5VDUAL分壓)	-USBOC_R
GPO[16]	OUTPUT	VCC3	-GNT[6]	(integrated VCC3)	Reserved
GPO[17]	OUTPUT	VCC3	-GNT[5]	(integrated VCC3)	Reserved
GPO[18]	OUTPUT	VCC3	GPO[18]	(P.U VCC3)	LANRST-
GPO[19]	OUTPUT	VCC3	GPO[19]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[20]	OUTPUT	VCC3	GPO[20]	(P.U VCC3)	TBL-
GPO[21]	OUTPUT	VCC3	GPO[21]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[22]	Not Implemented		Not Implemented		Not Implemented
GPO[23]	OUTPUT	VCC3	GPO[23]	(P.U VCC3)	LANRST-
GPO[24]	IN/OUT	3VDUAL	GPO[24]	(NA)	GREEN_LED
GPO[25]	IN/OUT	3VDUAL	vcc_25vregulator	(NA)	Reserved
GPI[26]	Input	VCC3	SATA[0]GP	(P.U VCC3)	SATA[0]GP
GPIO[27]	IN/OUT	3VDUAL	GPIO[27]	(NA)	Reserved
GPIO[28]	IN/OUT	3VDUAL	GPO[28]	(NA)	PWD_LED
GPI[29]	Input	VCC3	SATA_1GP	(P.U VCC3)	SATA_1GP
GPI[30]	Input	VCC3	SATA_2GP	(P.U VCC3)	SATA_2GP
GPI[31]	Input	VCC3	SATA_3GP	(P.U VCC3)	SATA_3GP
GPIO[32]	IN/OUT	VCC3	GPO[32]	(NA)	FWP-
GPIO[33]	IN/OUT	VCC3	GPI[33]	(P.U VCC3)	-ACZ_DET
GPIO[34]	IN/OUT	VCC3	GPIO[34]	(P.U VCC3)	MB_ID0
GPI[40]	Input	V5REF	-REQ[4]	(P.U VCC)	-REQ[4]
GPI[41]	Input	VCC3	GPI[41]	(P.U VCC3)	MB_ID1
GPO[48]	OUTPUT	VCC3	-GNT[4]	(integrated VCC3)	Reserved
GPO[49]	OD O	V_CPU_IO	CPUPWROK	(P.U VTT_OR)	CPUPWROK
GP1O[35-39,42-47]	NOT IMPLEMENTED		NOT IMPLEMENTED		

GPO PIN

Pin Name	Pin Number	Power Well	Pin Type			GPIO Application

GIGABYTE

Title	GPIO TABLE	
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ICH6 GPIO Table:

NAME	PWR LANE	USAGE	NAME	PWR LANE	USAGE
GPI0	V5REF	M/B ID (-REQ6)	GPI41	VCC3	M/B ID
GPI1	V5REF	-REQ5	GPO48	VCC3	-GNT4
GPI2	V5REF	-PIRQE	GPO49	V-CPUIO	CPUPWOK
GPI3	V5REF	-PIRQF			
GPI4	V5REF	-PIRQG			
GPI5	V5REF	-PIRQH			
GPI6	VCC3	-SLP BTN			
GPI7	VCC3	DUAL BIOS			
GPI8	3VDAUL	-LANWAKE			
GPI9	3VDAUL	-USBOC4			
GPI10	3VDAUL	-USBOC5			
GPI11	3VDAUL	-SMBALT			
GPI12	VCC3	ATX DET			
GPI13	3VDAUL	-LPCPME			
GPI14	3VDAUL	-USBOC6			
GPI15	3VDAUL	-USBOC7			
GPO16	VCC3	CPU OV1 (-GNT6)			
GPO17	VCC3	-GNT5			
GPO18	VCC3	CPU OV2			
GPO19	VCC3	DUAL BIOS			
GPO20	VCC3	BIOS T-BLOCK			
GPO21	VCC3	DUAL BIOS			
GPO23	VCC3	DDR OV0			
GPIO24	3VDAUL	GREEN LED			
GPIO25	3VDAUL	DDR OV1			
GPI26	VCC3	SATA_GP0			
GPIO27	3VDAUL	+PWRLED			
GPIO28	3VDAUL	-PWRLED			
GPI29	VCC3	SATA GP1			
GPI30	VCC3	SATA GP2			
GPI31	VCC3	SATA GP3			
GPIO32	VCC3	BIOS WP			
GPIO33	VCC3	AZALIA DET			
GPIO34	VCC3	M/B ID			
GPI40	V5REF	-REQ4			

PWROK/RESET Table:

ITE8712BHX PIN	NET NAME	TARGET
PIN62/-PCIRST1	-PCIE_RST	1. PCI-E * 1 Slot1 2. PCI-E * 1 Slot2 3. PCI-E * 1 Slot3 4. PCI-E * 16 Slot
PIN64/-PCIRST2	-PFMRST2	1. Onboard PCI Lan 2. Onboard 1394 Chip 3. OnBoard FWH
PIN65/-PCIRST3	-PFMRST1	1. Onboard PCI-E Lan 2. Onboard SATA Chip 3. GMCH
PIN115/-PCIRST4	-PFMRST_ -IDERST	Reserved For IDE
PIN63/PWROK1	PWROK1	1. GMCH 2. ICH6 3. 5VDUAL SWITCH 4. DPS CONTROL
PIN109/PWROK2	-THERM	1. ICH6

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Title: GPIO/RESET TABLE

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